N32H765 Product Brief

The N32H765 series uses an ARM Cortex-M7 core, running at frequencies up to 600MHz, supporting double-precision floating-point operations and DSP instructions. It features (2/4MB) on-chip FLASH, integrates up to 1504KB of SRAM (including 1024KB TCM SRAM and 480KB SRAM) + 4KB Backup SRAM. It includes 3 12-bit 5Msps ADCs, 4 high-speed comparators, 6 12-bit DACs, and integrates multiple high-speed communication interfaces: U(S)ART, I2C, xSPI, SPI, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, and 10/100/1000M Ethernet.

The series supports digital camera interface (DVP), TFT-LCD graphical interface, JPEG hardware codec and GPU. It features a built-in high-performance encryption algorithm hardware acceleration engine, supporting AES/TDES, SHA、SM4 algorithms, TRNG true random number generator, and CRC8/16/32. It supports up to 126 GPIOs, and is available in LQFP144 、LQFP176 and BGA176+25 packages.

Key Features

- **Core CPU**
  - 32-bit ARM Cortex-M7 core, double-precision floating-point unit, supports DSP instructions and MPU
  - Built-in 32KB instruction Cache and 32KB data Cache with ECC
  - Maximum frequency 600MHz, 1284 DMIPS
- **Encrypted Memory**
  - On-chip Flash (2/4MB), supports encrypted storage and automatic program decryption during execution
  - 1504KB built-in SRAM, supports ECC verification
    - 1024KB TCM SRAM, configurable as D-TCM, I-TCM or SRAM
    - 480KB on-chip SRAM
  - 4KB Backup SRAM, supports ECC
- **Operating Modes**
  - Run mode
  - SLEEP mode: AXI enabled, AHB enabled
  - Stop0 mode: SRAM, TCM, RTC, LSE, IWDG enabled
  - Stop2 mode: Flash standby mode, SRAM, TCM, RTC, LSE, IWDG, Backup SRAM, backup registers enabled, I/O maintained
  - Standby mode: Backup SRAM, RTC, IWDG, LSE, backup registers enabled, SRAM, TCM disabled
  - VBAT mode: Backup SRAM, RTC, LSE, backup registers enabled
- **Clock**
  - 4MHz~48MHz external high-speed crystal
  - 4MHz~50MHz external clock input

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- 32.768KHz external low-speed crystal
- Built-in 3 high-speed PLLs
- Built-in MSI clock, supporting configuration of 31.25K/62.5K/125K/250K/500K/1M/2M/4M/8M/16MHz clocks
- Internal high-speed RC 64MHz
- Internal low-speed RC 32KHz

- **Reset**
  - Supports power-on/power-down/external pin reset
  - Supports watchdog reset and software system reset
  - Supports programmable voltage detection
- **High-Speed Communication Interfaces**
  - 7 USART interfaces/6 UART interfaces, supporting ISO7816, IrDA, LIN
  - 2 LPUART interfaces
  - 6 SPI interfaces, supporting master/slave modes, rates up to 50 MHz
  - 8 I2C interfaces, rates up to 3.4 MHz, configurable master/slave modes, dual address response in slave mode
  - 2 USBHS Dual Role interfaces
  - 8 CAN-FD bus interfaces
  - 2 Ethernet MAC interface, ETH1 suppors 10M/100M/1000M communication rates, ETH2 supports 10M/100M communication rates . Supports IEEE 1588 time synchronization protocol
- High-Performance Analog Interfaces
  - 3 12-bit 5Msps ADCs, supporting 12-bit, 10-bit resolution, hardware oversampling up to 16-bit, supporting single-ended and differential modes
  - 4 high-speed analog comparators
  - 6 12-bit DACs, of which 2 1Msps DACs support output with or without Buffer separately, internal output only supports mode without Buffer; simultaneous internal and external output must enable Buffer; the other 2 DACs only support 1 output channel to the internal chip, with 15Msps sampling rate, supporting internal output without Buffer
  - 2 MCO outputs, configurable to output SYSCLK, HSE, MSI, LSE, LSI, HSI64 or PLL clock division
  - Supports 1 reference voltage VREFBUF (configurable as 1.5V/1.8V/2.048V/2.5V)
  - 1 temperature sensor
- **Audio Interfaces**
  - 4 I2S, supporting master/slave modes, audio sampling frequencies from 8KHz to 192KHz
  - 8 PDM digital microphone interfaces built into DSMU
- **Memory Extension Interfaces**
  - 1 FEMC (Flexible External Memory Controller) interface, bus rate 100 MHz, SRAM/PSRAM/Nor Flash supporting configurable 16/32-bit data width, NAND Flash supporting configurable 8/16-bit data width

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- 1 xSPI interface, supporting 1/2/4/8-bit data width, configurable master/slave, rates up to 133 MHz, can be used for external SRAM, PSRAM and Flash, supports XIP
- 1 SDRAM interface, rates up to 133 MHz
- 2 SDMMC interfaces, supporting SD/SDIO 3.0, eMMC 4.51 format, rates up to 104MHz

- **Image Processing Interfaces**
  - 2 digital camera interface (DVP), supporting 8/10/12/16bit, rates up to 110MHz
  - 1 TFT-LCD display interface, supporting up to 24-bit parallel digital RGB LCD, providing all signal interfaces, can directly connect to various LCD and TFT panels, resolution up to 1920x1080
  - Built-in 2.5D graphics processor, supporting image scaling, rotation, blending, anti-aliasing, texture mapping, etc.
  - Hardware JPEG codec
- **Maximum support for 126 GPIOs, low-speed GPIOs support 5V tolerance (under VDD = 3.3V ±10% conditions)**
- **Motor control Cordic accelerator, supporting trigonometric and hyperbolic function acceleration, supporting floating-point input and output**
- **Delta Sigma Module Unit (DSMU)**
- **Built-in filtering algorithm accelerator FMAC, supporting FIR, IIR filtering**
- **3 high-speed DMA controllers, each controller supporting 8 channels, 1 MDMA supporting 16 channels, freely configurable channel source and destination addresses**
- **RTC real-time clock, supporting leap year perpetual calendar, alarm events, periodic wake-up, supporting internal and external clock calibration**
- **Timer Counters**
  - 2 16bit super high-resolution timer (SHRTIM1/ SHRTIM2). Supports maximum control precision of 100ps, Each super high-resolution timer counter consists of 1 master timer unit and 6 16-bit slave timer units. each timer unit has 2 independent channels. Supports 12 independent PWM outputs or 6 pairs of complementary PWM outputs.
  - 3 16-bit advanced timer counters, supporting input capture, complementary output, quadrature encoding input and other functions, highest control precision 3.3ns; each timer has 6 independent channels, of which 4 channels support 4 pairs of complementary PWM outputs
  - 10 16-bit general-purpose timers (GTIMA1~GTIMA7, GTIMB1~ GTIMB3), each timer with 4 independent channels, supporting input capture, output compare, PWM generation
  - 4 32-bit basic timer counters (BTIM1~4)
  - 5 16-bit low-power timers (LPTIM1~5), can work in Stop2 mode
  - 1x 24-bit SysTick, 1x 14-bit window watchdog (WWDG), 1x 12-bit independent watchdog (IWDG)
- Programming Methods
  - Supports SWD/JTAG online debugging interface

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- Supports USB, UART Bootloader

- Security Features
  - FLASH has up to 4 encryption partitions, supporting storage encryption
  - Supports write protection (WRP), multiple levels of read protection (RDP) (L0/L1/L2)
  - Built-in password algorithm hardware acceleration engine, supporting AES/TDES, SHA, algorithms
  - TRNG true random number generator, CRC8/16/32 operations
  - Supports secure boot, encrypted program download, secure update, supports external high-speed and low-speed clock failure detection
  - Supports tamper detection
- **OTP supports 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range:
    - 2.3V~3.6V
    - Chip junction temperature range: -40°C~125°C
- **Security Features**
  - USB IF
  - IEC61508 SIL2
- **Security Features**
  - LQFP144(20mm x 20mm)
  - LQFP176(24mm x 24mm)
  - BGA176+25(10mm x 10mm)
- **Ordering Models**

Series	Models
N32H765xxx7	N32H765ZKL7, N32H765ZIL7, N32H765IKL7, N32H765IIL7, N32H765IKB7, N32H765IIB7

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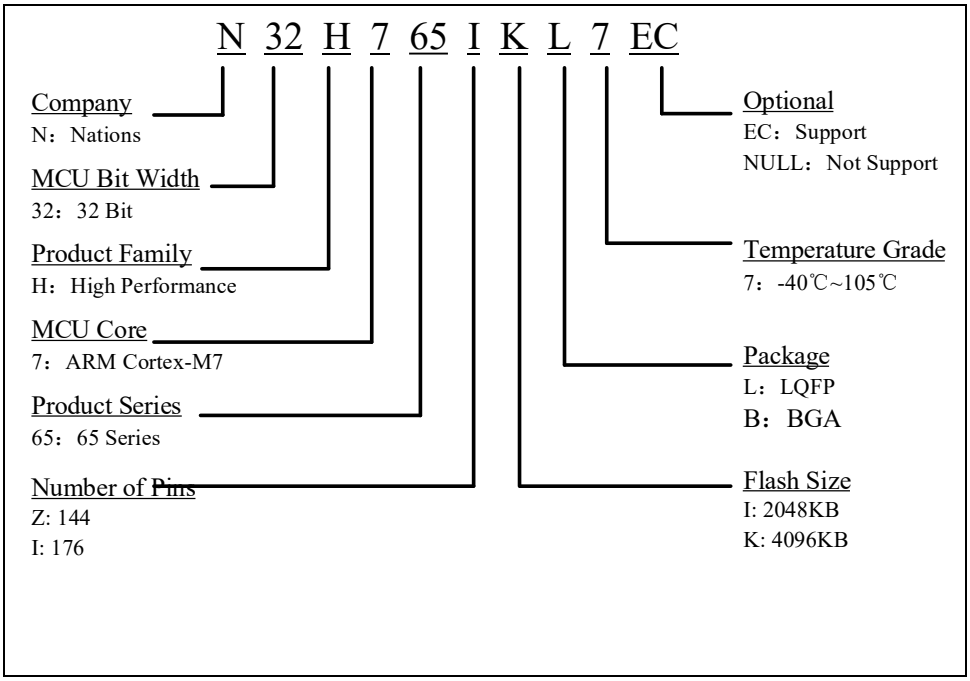
1 Naming Convention



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2 Device Overview

Table 2-1 N32H765 Series Resource Configuration

Device Model		N32H765 ZKL7	N32H765 ZIL7	N32H765 IKL7	N32H765 IIL7	N32H765 IKB7	N32H765 IIB7
Flash（KB）		4096	2048	4096	2048	4096	2048
SRAM（KB）	TCM	1024(1)					
	System RAM	480					
	Backup RAM	4					
Core	M7	600MHz					
Operating Voltage		2.3V~3.6V					
DCDC(step-down)		Yes					
Co-processor	Cordic	Yes					
	DSMU	Yes					
	FMAC	Yes					
Timers	SHRTIM	2					
	ADTIM	2*16bit(2)		3*16bit(2)			
	GPTIM	10*16bit					
	BSTIM	4*32bit					
	LPTIM	5*16bit					
	SysTick timer	1					
	WWDG	1*14bit					
	IWDG	1*12bit					
	RTC	Yes					
Communication Interfaces	SPI/I2S	6/4(3)					
	I2C	8(4)					
	USART	5(5)		7(5)			
	UART	5(6)		6(6)			
	LPUART	2					
	USBHS Dual Role	2					
	CAN FD	7(7)		8(7)			
	10/100M ETH	1(8)		2(8)			
	10/100/1000M ETH	-		1(8)			
Extended memory	SDRAM	-		Yes			
	xSPI	1(9)					
	FEMC	Yes					
	SDMMC	2					
Analog	12bit ADC Number of channels	3 23		3 28		3 36	
	12bit DAC Number of channels	2+4(10) 2 External channels					
	Comparators	2(11)		3(11)		4(11)	
	VREFBUF	Yes					

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Imaging	LCDC	Yes		
	GPU	Yes		
	JPEG	Yes		
	DVP	1	2	
GPIO		99	121	126
DMA Number of channels		3 24Channel		
MDMA Number of channels		1 16Channel		
Algorithm support		DES/3DES, AES, SHA1/SHA224/SHA256, CRC8/16/CRC32		
Security Protection		Read/write protection (RDP/WRP), storage encryption, secure boot		
Packages		LQFP144 (20mm x 20mm)	LQFP176 (24mm x 24mm)	BGA176+25 (10mm x 10mm)

Note：

1. SRAM is the default upon power-on, and users can independently configure the sizes of ITCM, DTCM and SRAM.
2. Description of ATIM interface: 2 stands for ATIM1~2, and 3 stands for ATIM1~3.
3. SPI interfaces include SPI1~6, and I2S interfaces include I2S1~4.
4. I2C interfaces include I2C1~8.
5. Description of USART interface: 5 stands for USART1~5, and 6 stands for USART1~6.
6. Description of UART interface: 5 stands for UART9~13, and 6 stands for UART9~14.
7. Description of FDCAN interface: 7 stands for FDCAN1~7, and 8 stands for FDCAN1~8.
8. Description of ETH interface: 1 means supporting ETH1; 2 means supporting ETH1~2; ETH1 supports 10M/100M/1000M, and ETH2 supports 10M/100M.
9. The xSPI interface is xSPI2.
10. The 4 DACs only support internal connection and cannot output to GPIOs.
11. Description of COMP interface: 2 stands for COMP1~2, 3 stands for COMP1~3, and 4 stands for COMP1~4.

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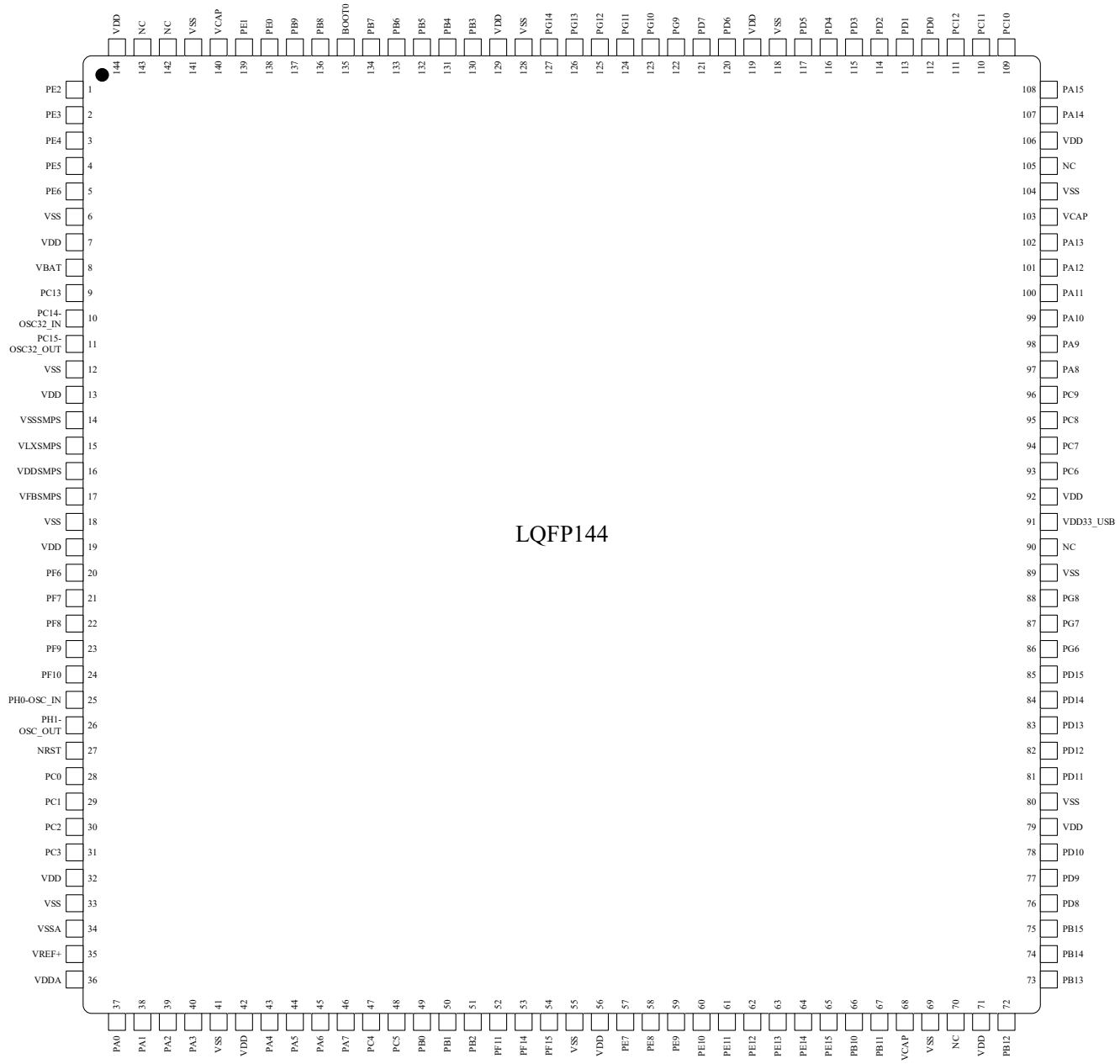
3 Package Information

3.1 LQFP144 Package

3.1.1 LQFP144 Pin Distribution



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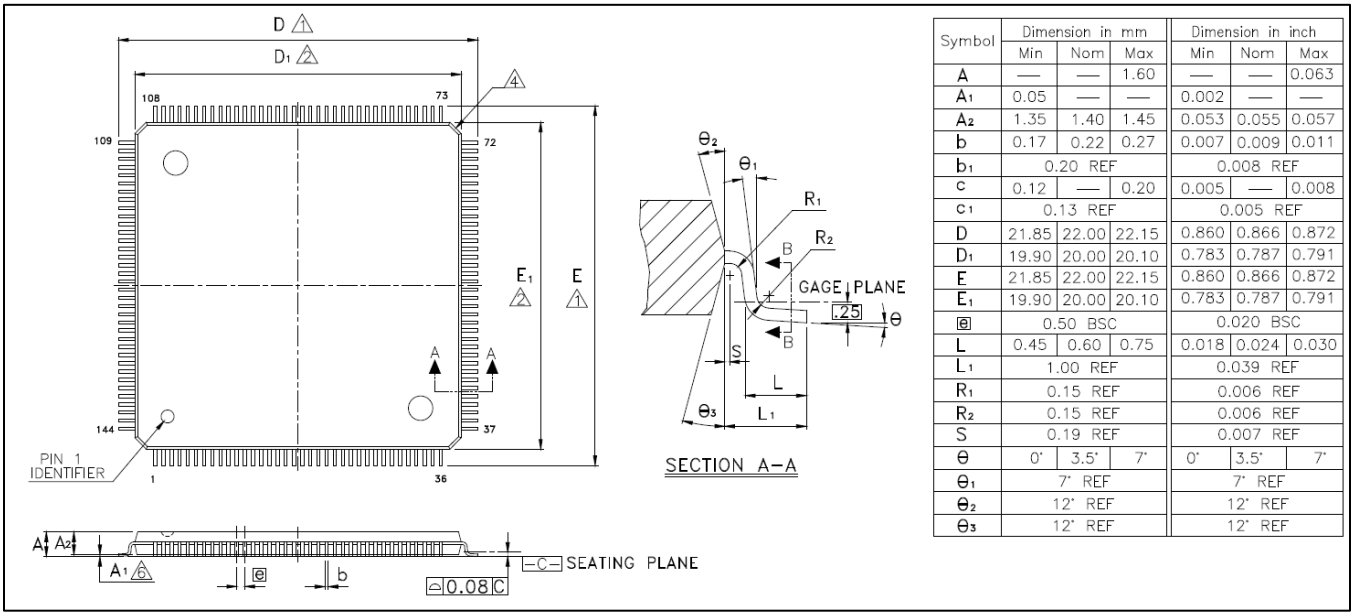
3.1.2 LQFP144 Package Size



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.20 REF			0.008 REF		
c	0.12	—	0.20	0.005	—	0.008
c_1	0.13 REF			0.005 REF		
D	21.85	22.00	22.15	0.860	0.866	0.872
D_1	19.90	20.00	20.10	0.783	0.787	0.791
E	21.85	22.00	22.15	0.860	0.866	0.872
E_1	19.90	20.00	20.10	0.783	0.787	0.791
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.15 REF			0.006 REF		
R_2	0.15 REF			0.006 REF		
S	0.19 REF			0.007 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	7° REF			7° REF		
$θ_2$	12° REF			12° REF		
$θ_3$	12° REF			12° REF		

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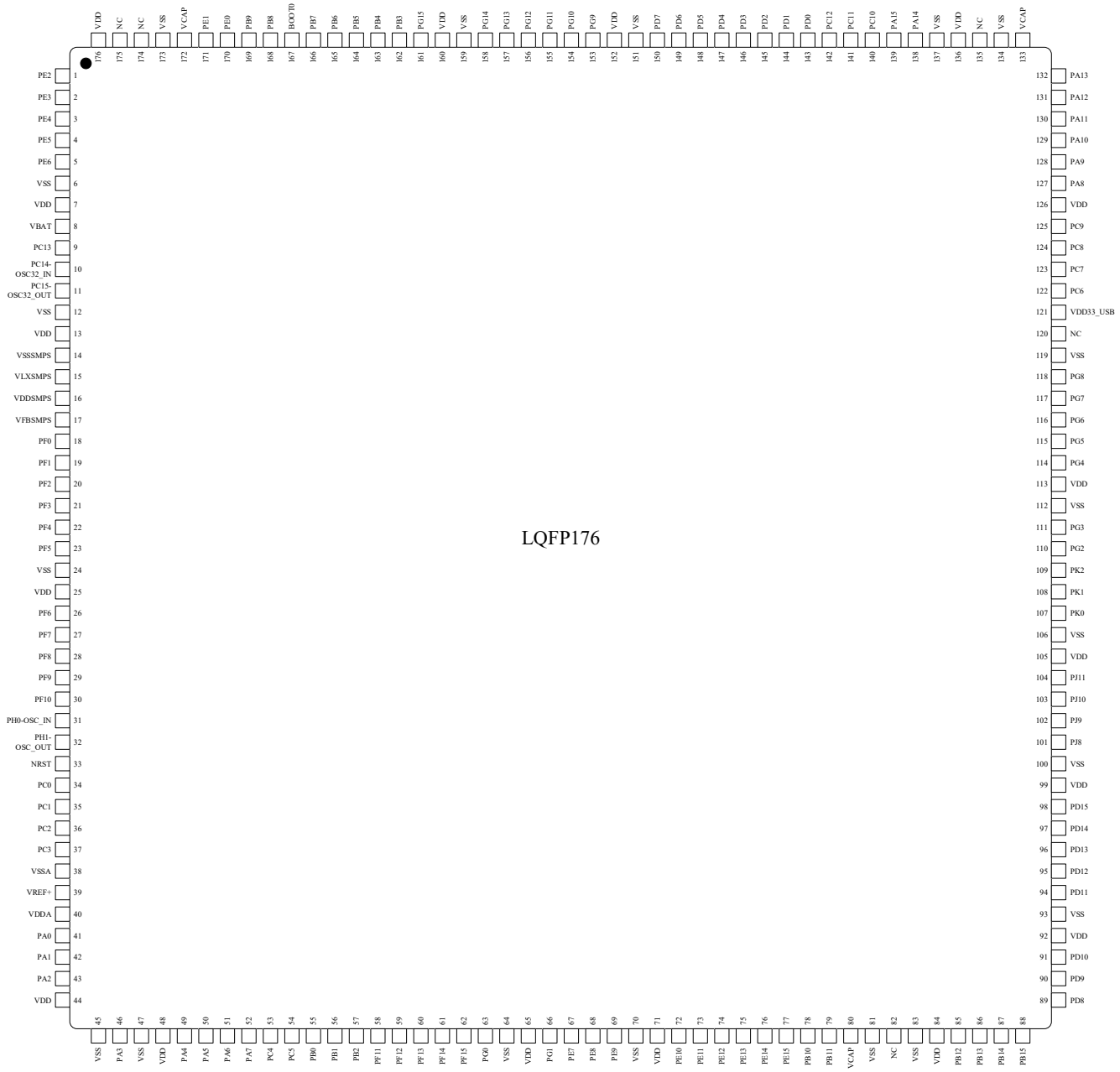
3.2 LQFP176 Package

3.2.1 LQFP176 Pin Distribution



LQFP176

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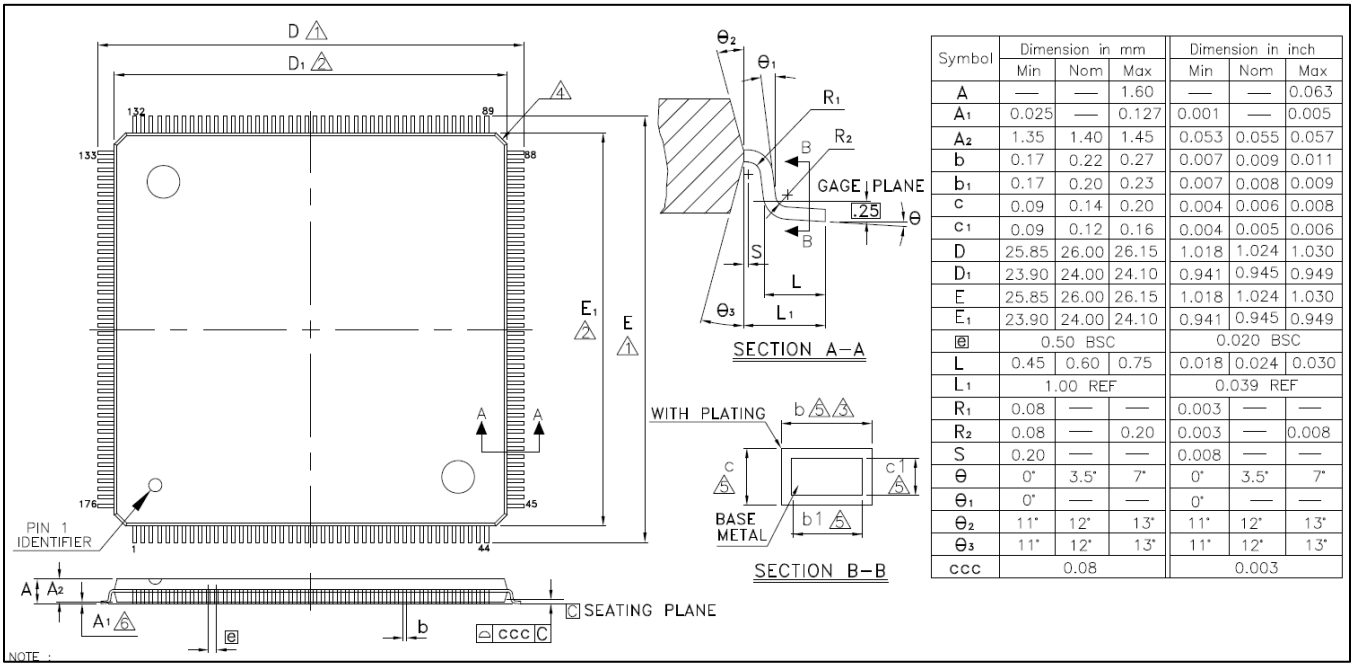
3.2.2 LQFP176 Package Size



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.025	—	0.127	0.001	—	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	0.14	0.20	0.004	0.006	0.008
c1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

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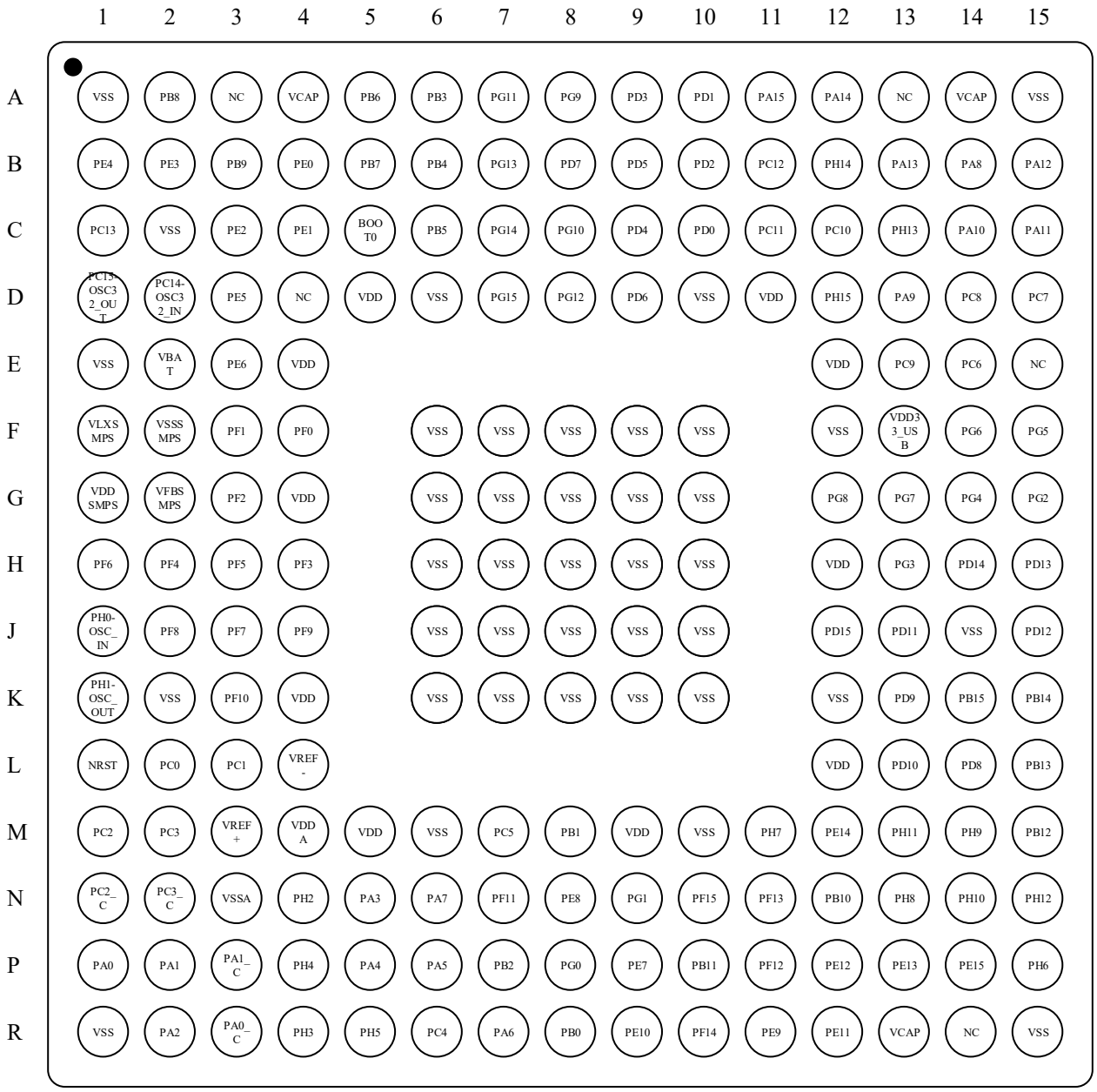
3.3 BGA176+25 Package

3.3.1 BGA176+25 Pin Distribution



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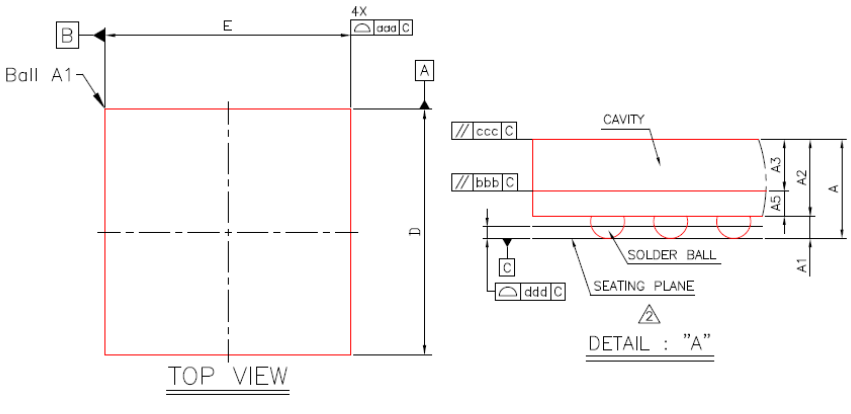
3.3.2 BGA176+25 Package Size



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0,919	1,000	1,081	0,036	0,039	0,043
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.726	0.790	0.854	0.029	0.031	0.034
A3	0.480	0.530	0.580	0.019	0.021	0.023
A5	0.220	0.260	0.300	0.009	0.010	0.012
E	9.900	10.000	10.100	0.390	0.394	0.398
D	9.900	10.000	10.100	0.390	0.394	0.398
E1	—	9.100	—	—	0.358	—
D1	—	9.100	—	—	0.358	—
e	—	0.650	—	—	0.026	—
b	0.260	0.310	0.360	0.010	0.012	0.014
aaa		0.150			0.006	
bbb		0.100			0.004	
ccc		0.100			0.004	
ddd		0.100			0.004	
eee		0.150			0.006	
fff		0.080			0.003	
MD/ME		15/15				
SE		0.650			0.026	
SD		0.650			0.026	

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc & ddd (SPIL STANDARD).
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. BALL PLACEMENT USE 0.300 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.275 mm.

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4 Version History

Version	Date	Changes
V1.1.0	2025.10.17	First release

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