N32A455xxL7 Datasheet

N32A455xxL7 series based on 32-bit ARM Cortex-M4F kernel, run up to 144MHz, support floating-point unit and DSP instructions, up to 512KB embedded flash, 144KB SRAM, 4x12bit 4.7Msps ADC, 4xOPAMP, 7xCOMP, 2x1Msps 12bit DAC. Integrates multi-channel U(S)ART, I2C, SPI, QSPI and CAN communication interfaces, 1x SDIO interface and built-in cryptographic algorithm hardware acceleration engine.

Key features

- **CPU core**
  - 32-bit ARM Cortex-M4 +FPU, one-cycle hardware multiply instructions, DSP instruction and MPU support
  - Built-in 8KB instruction Cache, which support Flash acceleration unit to execute program 0 wait
  - Run up to 144MHz, 180DMIPS
- **Encrypted memory**
  - Up to 512K Bytes of embedded Flash memory, supporting encrypted storage, multi-user partition management and data protection, hardware ECC check, 100,000 cycling and 10 years data retention
  - 144K Bytes of SRAM (including 16K Byte Retention RAM), Retention RAM supporting hardware parity check
- **Clock**
  - HSE: 4MHz~32MHz External high-speed crystal
  - LSE: 32.768KHz External low-speed crystal
  - HSI: Internal high-speed RC OSC 8MHz
  - LSI: internal low-speed RC OSC 40KHz
  - Built-in high speed PLL
  - MCO: Support 1-way clock output, configurable SYSCLK, HSE, HSI or PLL clock output that can be divided
- **Reset**
  - Support power-on/power-down/ brown-out/external pin reset
  - Support programmable low-voltage detection and reset
  - Support watchdog reset, software reset
- **Communication interface**
  - Up to 7x U(S)ART interfaces up to 4.5 Mbps, including 3x USART interfaces (supporting ISO7816, IrDA, LIN), and 4x UART interfaces
  - 3x SPI interfaces up to 36 MHz, two of which support I2S
  - 1x QSPI interface up to 144 Mbps
  - 4x I2C interfaces up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
  - 2x CAN 2.0A/B bus interfaces
  - 1x SDIO interface supporting SD/SDIO/MMC format
- **High-performance analog interface**

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- 4x 12-bit 4.7Msps high-speed ADC, 12/10/8/6bit configurable, 6bit mode up to 8.9Msps sampling rate, up to 38 external single-ended input channels, supporting differential mode.
- 4x rail-to-rail operational amplifiers with built-in up to 32x programmable gain amplification
- Up to 7x high-speed analog comparators with built-in 64-level adjustable reference
- 2x 12-bit DAC with sampling rate of 1Msps
- External input independent reference voltage source
- All analog interfaces support 1.8~3.6V full voltage operation.

- **Up to 80 GPIOs supporting multiplexing function are supported, and most GPIOs support 5V tolerant**
- **2x high-speed DMA controllers, each controller supports eight channels, and channel source address and destination address can be configured arbitrarily**
- **1x RTC real-time clock, supporting leap year perpetual calendar, alarm events, periodic wake-up, and internal and external clock calibration.**
- **Timer counter**
  - 2x 16-bit advanced timer counters, support input capture, complementary output, orthogonal encoding input, maximum control accuracy 6.9ns. Each timer has four independent channels, three of which supports 3 channels and 6 complementary PWM output.
  - 4x 16-bit general-purpose timer counters, each timer has 4 independent channels, support input capture/output comparison/PWM output/one-pulse output.
  - 2x 16-bit basic timing counters
  - 1x 24bit SysTick
  - 1x 7bit Window Watchdog (WWDG)
  - 1x 12bit Independent Watchdog (IWDG)
- **Programming mode**
  - Support SWD/JTAG online debugging interface
  - Support UART Bootloader
- **Safety features**
  - Built-in cryptographic algorithm hardware acceleration engine
  - DES/3DES、AES、SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7 and MD5 algorithms are supported.
  - Flash storage encryption
  - Multi-user partition management (MMU)
  - TRNG true random number generator
  - CRC16/32
  - Support write protection (WRP) and multiple read protection (RDP) levels (L0/L1/L2)
  - Support secure startup, encrypted download of programs, and secure update.
  - Support external clock failure detection, tamper detection.
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Voltage range: 1.8V~3.6V
  - Working temperature range: -40 ℃ ~105 ℃

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- Passed AEC-Q100-G2 certification
- ESD: ±4KV (HBM model), ±1KV(CDM model)

- **Encapsulation**
  - LQFP48(7mm x 7mm)
  - LQFP64(10mm x 10mm)
  - LQFP100(14mm x 14mm)

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1 Product introduction

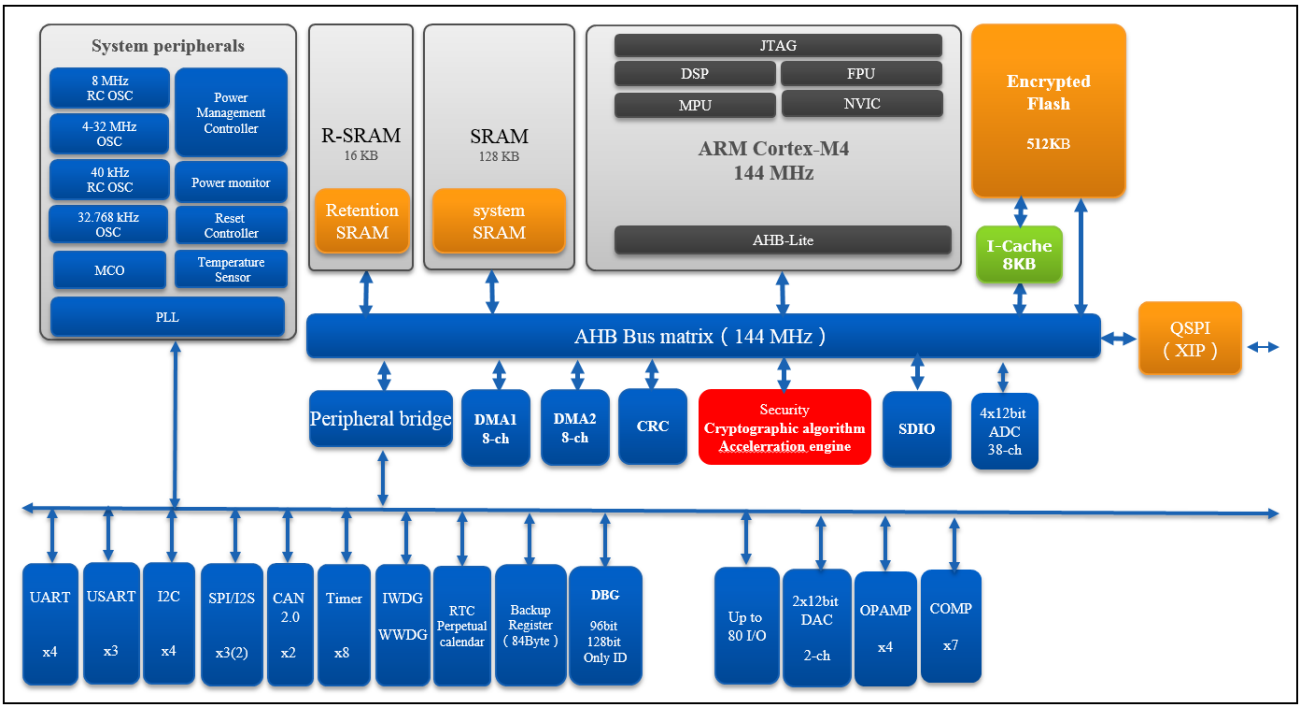
N32A455xxL7 family of microcontrollers features a high-performance 32-bit ARM Cortex™-M4F core, integrate floating point operation unit (FPU) and Digital Signal Processing (DSP), and support parallel computing instructions. Maximum operating frequency is 144MHz, integrated up to 512KB encrypted storage Flash and supports multi-user partition management, maximum 144KB of embedded SRAM. Built-in one internal high-speed AHB bus, two low-speed peripheral clock buses APB and bus matrix, supporting up to 80 general I/O. Provide abundant high-performance analog interfaces, including 4x 12-bit 5Msps ADC, up to 38 external input channels, 2x 1Msps 12-bit DAC, 4x independent rail-to-rail operational amplifiers, up to 7 high-speed comparators interfaces. It provide a variety of digital communication interfaces, Including 7x U(S)ART, 4x I2C, 3x SPI, 2x I2S, 1x QSPI, 2x CAN 2.0B, 1x SDIO communication interface. Built-in cryptographic algorithm hardware acceleration engine, supports hardware acceleration of a variety of international and national cryptographic algorithms.

N32A455xxL7 series products can work stably in the temperature range of -40 ℃ to +105 ℃, supply voltage from 1.8V to 3.6V, provides a variety of power modes for users to choose from, meeting the requirements of low-power applications. This series of products is available in 4 different packaging forms from 48 pins to 100 pins. Depending on the package form, the peripheral configuration in the device varies.

These rich peripheral configurations make the car regulation N32A455xxL7 series microcontrollers suitable for car window controllers (door control; sunroof/sunshade control; electric tailgate control; electric pedal control), light controllers (AFS; atmosphere light control), air conditioning control systems (HVAC; new energy vehicle PTC; commercial vehicle PTC; commercial vehicle SCR) Various application scenarios of on-board motor controller (electronic water pump; electronic fuel pump; commercial vehicle urea pump) and others (TPMS; receiver; seat control; reversing radar; instrument monitoring MCU; EDR).

Figure 1-1 the block diagram of this series of products is given.

Figure 1-1 Block diagram of N32A455xxL7 series



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1.1 List of devices

Table 1-1 N32A455xxL7 Series Resource Configuration

Part number		N32A455CEL7	N32A455REL7	N32A455VEL7
Flash(KB)		512		
SRAM(KB)		144		
CPU frequency		ARM Cortex-M4 @144MHz,180DMIPS		
Operating Voltage & temperature		1.8~3.6V/-40~105℃		
Timer	General	4		
	Advanced	2		
	Basic	2		
Communication interface	SPI	3		
	I2S	2		
	QSPI	Only Single Wire	1	
	I2C	3	4	
	USART	3		
	UART	3	4	
	CAN	2		
	SDIO	No	1	
GPIO		37	51	80
DMA		2		
Number of Channels		16Channel		
12bit ADC		4	4	4
Number of channels		16Channel	22Channel	38Channel
12bit DAC		2		
Number of channels		2Channel		
OPA/COMP		4/5	4/7	4/7
Algorithm support		DES/3DES、AES、 SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5、CRC16/CRC32、TRNG		
Security protection		Read-write protection (RDP/WRP), Storage encryption, Partition protection, Secure startup		
Package		LQFP48	LQFP64	LQFP100

1. SPI2 and SPI3 interfaces can flexibly switch between SPI mode and I2S audio mode.

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2 Function introduction

2.1 Processor core

N32A455xxL7 family integrates the latest generation of embedded ARM Cortex™-M4F processor, enhanced computing power based on the Cortex™-M3 core, new floating point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 1.25DMIPS/MHz. Its efficient signal processing capabilities are combined with the advantages of low power consumption, low cost, and ease of use of the Cortex-M family of processors to meet the requirements of a mixture of control and signal processing capabilities and easy to use applications.

ARM Cortex™-M4F 32-bit compact instruction set processor provides excellent code efficiency.

Note: Cortex™-M4F is backward compatible with Cortex-M3 code.

2.2 Storage

N32A455xxL7 series devices include embedded encrypted Flash memory and embedded SRAM. Figure 2-1 is a memory map.

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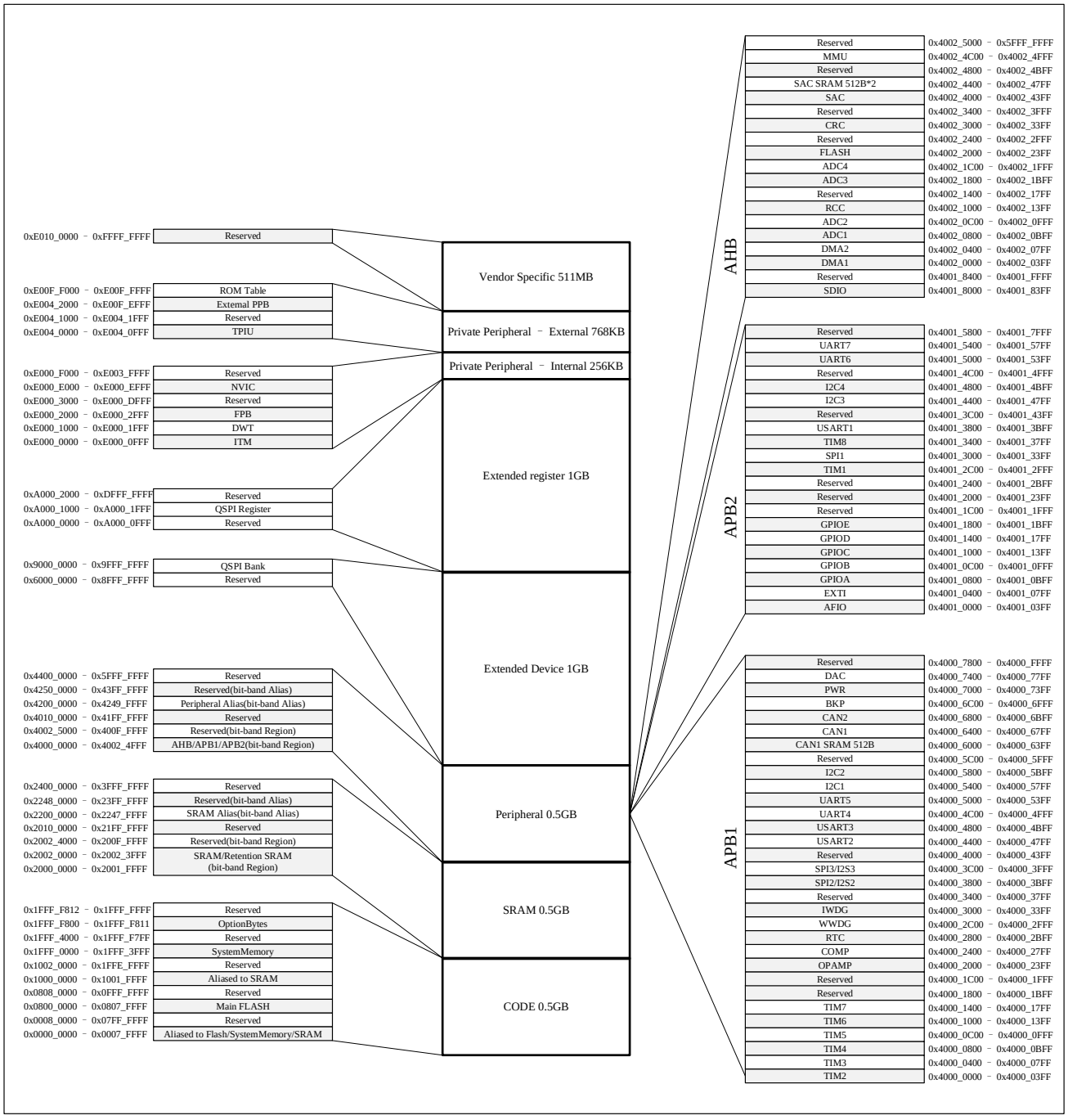
Figure 2-1 Memory map



2.2.1 Embedded flash memory

Integrated 512K bytes embedded encryption FLASH (FLASH), used to store programs and data, page size of 2Kbyte, supporting page erasing, word writing, word reading, half word reading, byte reading operations.

Support storage encryption protection, write automatic encryption, read automatic decryption (including program execution operation).

Support user partition management, can be divided into a maximum of two user partitions, different users cannot access each other's data (only executable code).

2.2.2 Embedded SRAM

Up to 144K bytes of built-in SRAM and R-SRAM are integrated on-chip, of which R-SRAM is Retention SRAM with a size of 16K bytes. R-SRAM supports Retention, which can retain data in STOP2 and Standby modes (can be

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configured to retain or not retain);

2.2.3 Nested vector interrupt controller (NVIC)

Built-in nested vector interrupt controller, capable of handling up to 86 maskable interrupt channels (not including the 16 Cortex™-M4F interrupts) and 16 priorities.

- Tightly coupled NVIC enables low latency interrupt response processing
- Interrupt vector entry address directly into the kernel
- Tightly coupled NVIC interface
- Allows early handling of interrupts
- Handles late arriving higher-priority interrupts
- Support interrupt tail link function
- Automatically saves processor state
- Automatically resumes when the interrupt returns with no additional instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.3 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 21 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured for its trigger event (rising or falling or both edges) and can be individually masked. There is a pending register that maintains the status of all interrupt requests. EXTI can detect that the pulse width is less than the clock period of the internal APB2. Up to 80 general purpose I/O ports are connected to 16 external interrupt lines.

2.4 Clock system

The device provides a variety of clocks for users to choose from, including internal high-speed RC oscillator HSI(8MHz), internal low-speed clock LSI(40KHz), external high-speed clock HSE(4MHz~32MHz), external low-speed clock LSE (32.768 KHz) and PLL.

During reset, the internal HSI clock is set as the default CPU clock, and then the user can choose the external HSE clock with failure monitoring function. When an external clock failure is detected, it will be isolated, the system will automatically switch to HSI, and if interrupts are enabled, the software can receive the corresponding interrupt. Also, security interrupt management of the PLL clock can be adopted when needed (such as when an indirectly used external oscillator fails).

Multiple pre-dividers are used to configure the AHB frequency, high-speed APB(APB2) and low-speed APB(APB1) areas. AHB has a maximum frequency of 144 MHz, APB2 has a maximum frequency of 72 MHz and APB1 has a maximum frequency of 36MHz. Refer to Figure 2-2 Clock tree diagram.

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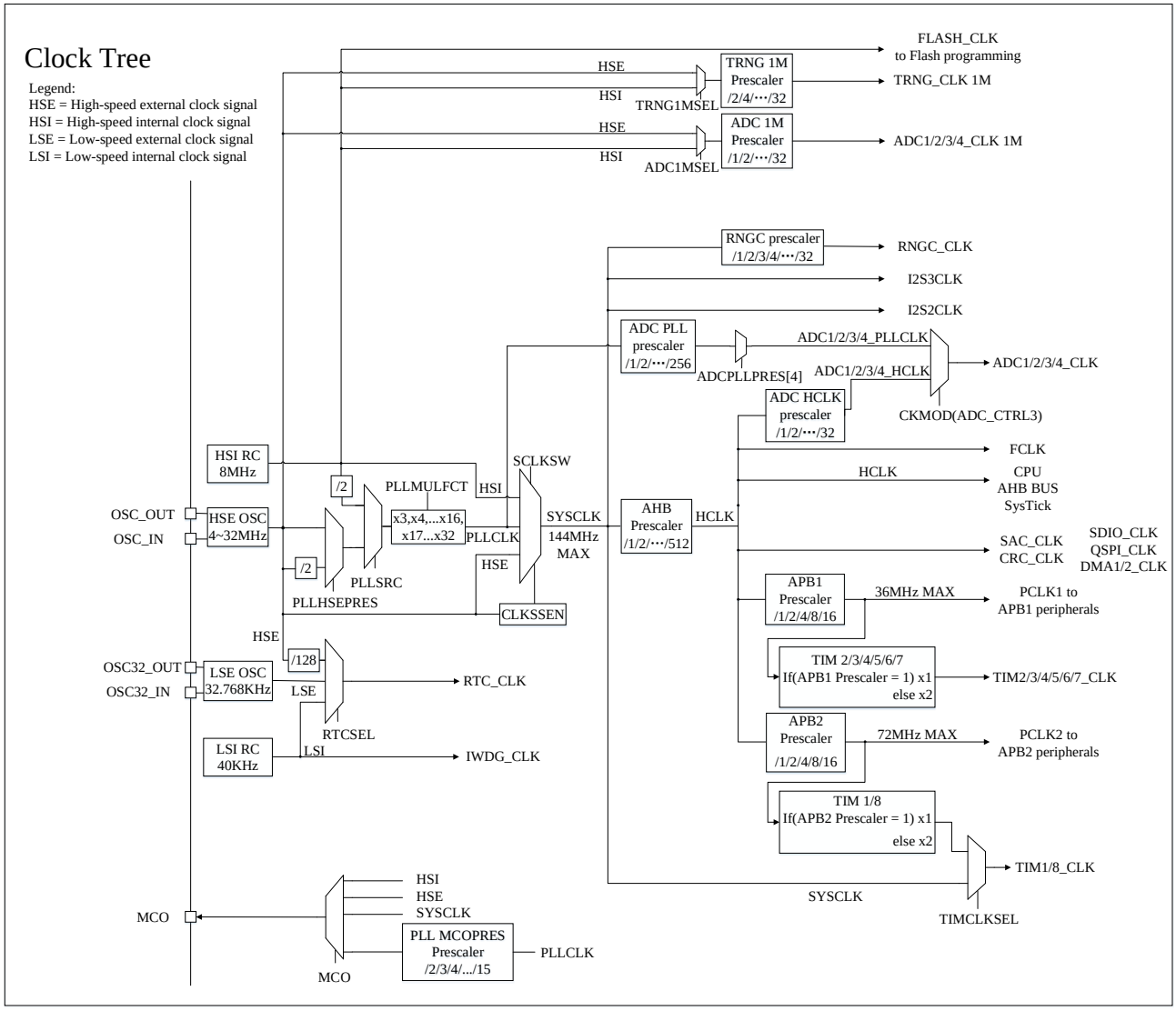
Figure 2-2 Clock tree



1. When HSI is used as the input of the PLL clock, the highest system clock frequency can only reach 128MHz.

2.5 Boot mode

At BOOT time, the BOOT mode after reset can be selected with the BOOT0/1 pin.

- BOOT from program FLASH Memory.
- BOOT from System Memory
- BOOT from internal SRAM

The Bootloader is stored in the system memory, and can program the flash memory through USART1 interface.

2.6 Power supply scheme

- V_{DD}= 1.8~3.6V, V_{DD} pin supplies power to the I/O pin and internal voltage regulator.
- V_{SSA}, V_{DDA}= 1.8~3.6V, provides power supply for ADC, DAC, OPAMP, COMP. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.
- V_{BAT}= 1.8~3.6V: When V_{DD} is turned off, it supplies power to RTC, external 32KHz oscillator and backup register.

For more information on how to connect the power supply pins, see Figure 4-3 Power supply scheme.

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2.7 Reset

The power-on reset (POR) and power-down reset (PDR) circuits are integrated inside. This part of the circuit is always in working state to ensure that the system works when the power supply exceeds 1.8V; when V_{DD} is lower than the set threshold ($V_{POR/PDR}$) , place the device in reset without using an external reset circuit.

2.8 Programmable voltage detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD}/V_{DDA} and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be started through the program. See Table 4-5 for values of $V_{POR/PDR}$ and V_{PVD}.

2.9 Voltage regulator

Voltage regulator operating modes as follow:

- MCU run in RUN, SLEEP modes: Main voltage regulator(MR) operates in normal mode
- MCU run in STOP0 modes: Main voltage regulator(MR) can select to operate in normal mode or in low power mode
- MCU run in STOP2, STANDBY mode: Main voltage regulator(MR) shut down and backup domain voltage regulator(BKR) turn on

After the chip is reset, the main voltage regulator(MR) operates in normal mode by default.

2.10 Low power mode

N32A455xxL7 series products support five low power consumption modes.

- SLEEP mode

In SLEEP mode, only the CPU stops and all peripherals are active and can wake up the CPU when an interrupt/event occurs.

- STOP0 mode

STOP0 mode is based on the Cortex-M4F deep sleep mode, which can achieve lower power consumption without losing the contents of the SRAM and registers. In STOP0 mode, most of the clocks of the main power domain are turned off, such as PLL, HSI, HSE, and the main voltage regulator can select to operate in normal mode or in low power mode.

Wake-up: The chip can be woken up from STOP0 mode by any signal configured as EXTI. The EXTI signal can be 16 external EXTI signals (I/O related), PVD output, RTC wake-up, RTC alarm clock.

- STOP2 mode

STOP2 mode is based on Cortex-M4F deep sleep mode, all core digital logic areas are powered off. The main voltage regulator is turned off and the HSE/HSI/PLL is turned off. CPU registers are maintained, LSE/LSI can be configured to work, all GPIOs are maintained, and peripheral I/O multiplexing functions are not maintained. 16K bytes R-SRAM is kept, other SRAM and register data will be lost. 84 bytes of backup register retention.

Wake-up: The chip can be woken up from STOP2 mode by any signal configured as EXTI. The EXTI signal can be 16 external EXTI signals (I/O related), PVD output, RTC periodic wake-up, RTC alarm clock, RTC invasion, NRST reset, IWDG reset.

- STANDBY mode

In STANDBY mode, the current consumption is low. Internal voltage regulator is turned off, PLL, HSI RC oscillator and HSE crystal oscillator are also turned off; after entering STANDBY mode, the content of the register will be lost, but the content of the backup register is still retained, R-SRAM can be maintained, Standby circuit still works.

An external reset signal on NRST, IWDG reset, a high level on the WKUP pin, or RTC's alarm can wake the microcontroller from STANDBY mode.

- VBAT mode

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At any time, whenever VDD is powered down, it will automatically enter VBAT mode. In VBAT mode, except NRST, PA0-WKUP, PC13_TAMPER, PC14, PC15, most I/O pins are in high impedance state.

Note: RTC, IWDG and corresponding clock will not be stopped when entering STANDBY mode.

2.11 Direct memory access (DMA)

The device integrates 2 flexible general-purpose DMA controllers, each DMA controller supports 8 channels, and can manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral data transfers; 2 DMA controllers support ring buffer management, which avoids the interruption of the controller transfer when it reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software at the same time. The length of the transfer, the source address and the destination address of the transfer can be individually set by software for each channel.

DMA can be used for major peripherals: SPI, I^2C, USART, advanced/generic/basic timers TIMx, DAC, I^2S, SDIO, ADC, QSPI.

2.12 Real time clock (RTC)

RTC is a set of continuously running counters with built-in calendar clock module, which can provide perpetual calendar function, as well as alarm clock interrupt and periodic interrupt (minimum 2 clock cycles) functions. RTC can be powered by V_{DD} or V_{BAT} pin. When V_{DD} is valid, select V_{DD} to supply power. Otherwise, it is powered by VBAT pin, which is automatically selected and switched by hardware. The RTC will not be reset by system or power reset sources, nor will it be reset when waking up from STANDBY mode.

The driving clock of RTC can be selected as 32.768KHz external crystal oscillator, internal low-power 40KHz RC oscillator, or any clock source divided by 128 for high-speed external clock. For application scenarios that require very high timing accuracy, it is recommended to use an external 32.768KHz clock as the clock source. At the same time, to compensate for the clock deviation of natural crystals, the RTC clock can be calibrated by outputting a 256Hz signal. The RTC has a 22-bit prescaler for the time base clock, by default when the clock is 32.768kHz it will produce a 1 second long time base. In addition, RTC can be used to trigger wake-up from low-power states.

2.13 Timer and watchdog

Up to 2 advanced control timers, 4 general-purpose timers and 2 basic timers, as well as 2 watchdog timers and 1 system tick timer.

The following Table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 2-1 Timer function comparison

Timer	Counter resolution	Counter type	Prescaler factor	Generate DMA request	Capture/compare channels	Complementary output
TIM1 TIM8	16 bits	Up, Down, Up/Down	Any integer between 1 and 65536	Y	4	Y
TIM2 TIM3 TIM4 TIM5	16 bits	Up, Down, Up/Down	Any integer between 1 and 65536	Y	4	N
TIM6 TIM7	16 bits	Up	Any integer between 1 and 65536	Y	0	N

2.13.1 Basic timer (TIM6 and TIM7)

Basic timers TIM6 and TIM7 each contain a 16-bit auto-reload counter.These two timers are independent of each other and do not share any resources.The basic timer can provide a time reference for general purpose timers.The basic timer is directly connected to the DAC inside the chip and drives the DAC directly through the trigger output.

The main functions of the basic timer are as follows:

- 16-bit auto-reload accumulating counter

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- 16-bit programmable prescaler (the frequency division factor can be configured as any value between 1 and 65536)
- Trigger DAC synchronization circuit
- Generate interrupt/DMA request on update event

2.13.2 General-purpose timer (TIMx)

4 general timers (TIM2, TIM3, TIM4 and TIM5) are mainly used in the following occasions: counting input signals, measuring the pulse width of input signals and generating output waveforms.

The main functions of the universal timer include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- TIM2, TIM3, TIM4 and TIM5 up to 4 channels.
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;
- Supports capture of internal comparator output signal.

2.13.3 Advanced control timer (TIM1 and TIM8)

The advanced control timers (TIM1 and TIM8) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Advanced timers have complementary output function with dead-time insertion and break function. Suitable for motor control.

The main functions of the advanced timer include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting).
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 up to 6 channels, TIM8 up to 6 channels
- 4 capture/compare channels, the working modes are PWM output, ouput compare, one-pulse mode output, input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture

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- Output compare
- Break input

- Complementary outputs with adjustable dead-time.
  - For TIM1 and TIM8, channel 1,2,3 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- TIM1_CC5 and TIM8_CC5 for COMP blanking.
- TIM1_CC6 is used to switch the input channel of OPAMP1 and OPAMP2; TIM8_CC6 is used to switch the input channel of OPAMP3 and OPAMP4;
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;

2.13.4 SysTick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a standard down counter.

It has the following characteristics:

- 24-bit down counter
- Automatic reload function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.13.5 Watchdog (WDG)

Support for two watchdog independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit decrepit counter and a 3-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP0, STOP2 and STANDBY modes. Once activated, if the dog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. The option byte can be configured to start the watchdog software or hardware. Reset and low power wake up are available.

Window Watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the decline counter value is flushed before the T6 bit becomes zero, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 7-bit decrement counter value (in the control register) is flushed before the decrement counter reaches the window register value, then an MCU reset will also occur. This indicates that the decrement counter needs to be refreshed in a finite time window.

Main features:

- WWDG is driven by the clock obtained by dividing APB1 clock
- Programmable free-running decrement counter
- Conditional reset:
  - When the decrement counter is less than 0x40, a reset is generated (if the watchdog is started)
  - A reset occurs when the decrement counter is reloaded outside the window (if the watchdog is started)

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- If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWINT) occurs when the decrement counter equals 0x40, which can be used to reload the counter to avoid WWDG reset

2.14 I²C bus interface

The device integrates up to 4 independent I2C bus interfaces, which provide multi-host function and control all I2C bus-specific timing, protocol, arbitration and timeout. Supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, System Management Bus(SMBus), and Power Management Bus(PMBus).

The main functions of the I2C interface are described as follows:

- Multi-master function: this module can be used as master device or slave device;
- I2C master device function:
  - Generate a clock;
  - Generate start and stop signals;
- I2C slave device function:
  - Programmable address detection;
  - I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode.
  - Stop bit detection;
- Generate and detect 7-bit / 10-bit addresses and broadcast calls;
- Support different communication speeds;
  - Standard speed (up to 100 kHz);
  - Fast (up to 400 kHz);
  - Fast + (up to 1MHz);
- Status flags:
  - Transmitter/receiver mode flag;
  - Byte transfer complete flag;
  - I2C bus busy flag;
- Error flags:
  - Arbitration is missing in Master mode
  - Acknowledge (ACK) error after address/data transfer;
  - Error start or stop condition detected
  - Overrun or underrun when clock extending is disable;
- Two interrupt vectors:
  - 1 interrupt for address/data communication success;
  - 1 interrupt for an error;
- Optional extend clock function
- DMA of single-byte buffers;
- Generation or verification of configurable PEC(Packet error detection)
- In transmit mode, the PEC value can be transmitted as the last byte
- PEC error check for the last received byte
- SMBus 2.0 compatible

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- Timeout delay for 25ms clock low
- 10 ms accumulates low clock extension time of master device
- 25 ms accumulates low clock extension time of slave device
- PEC generation/verification of hardware with ACK control
- Support address resolution protocol (ARP)

- PMBus compatible

2.15 Universal synchronous/asynchronous transceiver (USART)

N32A455xxL7 series products integrate up to 7 serial transceiver interfaces, including 3 universal synchronous/ asynchronous transceivers (USART1/USART2/USART3) and 4 universal asynchronous transceivers (UART4/ UART5/UART6/UART7). These 7 interfaces provide asynchronous communication, support for IrDA SIR ENDEC transmission codec, multi-processor communication mode, single-line half-duplex communication mode, and LIN master/slave function.

The communication rate of USART1/UART6/UART7 interface can reach 4.5Mbit/sec, and the communication rate of other interfaces can reach 2.25Mbit/sec.

The USART1, USART2 and USART3 interfaces have hardware CTS and RTS signal management, ISO7816-compatible smart card mode, and SPI-like communication mode, all of which can use DMA operations.

The main features of USART are as follows:

- Full duplex, asynchronous communication
- NRZ standard format
- Fractional baud rate generator system, baud rate programmable, used for sending and receiving, up to 4.5 Mbits/s
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates 13 bit interrupters and detects 10/11 bit interrupters
- Output sending clock for synchronous transmission
- IRDA SIR encoder decoder, supports 3/16 bit duration in normal mode
- Smart card simulation function
  - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3
  - 0.5 and 1.5 stop bits for smart cards
- Single-wire half duplex communication
- Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer
- Independent transmitter and receiver enable bits
- Detection flag
  - Receive buffer is full
  - Send buffer empty
  - End of transmission flag
- Parity control
  - Send parity bit
  - Verify the received data
- Four error detection flags

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- Overflow error
- Noise error
- Frame error
- Parity error

- 10 USART interrupt sources with flags
  - CTS change
  - LIN disconnect detection
  - Send data register is empty
  - Send complete
  - Received data register is full
  - Bus was detected to be idle
  - Overflow error
  - Frame error
  - Noise error
  - Parity the error
- Multi-processor communication, if the address does not match, then enter the silent mode;
- Wake up from silent mode (via idle bus detection or address flag detection)
- Mode configuration:

USART modes	USART1	USART2	USART3	UART4	UART5	UART6	UART7
Asynchronous mode	Y	Y	Y	Y	Y	Y	Y
Hardware flow control	Y	Y	Y	N	N	N	N
Multi-cache communication (DMA)	Y	Y	Y	Y	Y	Y	Y
Multiprocessor communication	Y	Y	Y	Y	Y	Y	Y
Synchronize	Y	Y	Y	N	N	N	N
Smart card	Y	Y	Y	N	N	N	N
Half duplex (single line mode)	Y	Y	Y	Y	Y	Y	Y
IrDA	Y	Y	Y	Y	Y	Y	Y
LIN	Y	Y	Y	Y	Y	Y	Y

2.16 Serial peripheral interface (SPI)

The device integrates 3 SPI interfaces, reusable as an I^2S interface, SPI shares resources with I^2S.

SPI allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner. This interface can be configured in master mode and provides a communication clock (SCK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-line simplex synchronous transmission using a two-way data line, and reliable communication using CRC checks.

The main functions of SPI interfaces are as follows:

- 3-wire full-duplex synchronous transmission
- Two-wire simplex synchronous transmission with or without a third bidirectional data line
- 8 or 16 bit transmission frame format selection
- Master or slave operations
- Support multi-master mode
- 8 master mode baud rate predivision frequency coefficient (maximum $f_{PCLK}/2$)
- Slave mode frequency (maximum $f_{PCLK}/2$)
- Fast communication between master mode and slave mode

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- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes
- Programmable clock polarity and phase
- Programmable data order, MSB before or LSB before
- Dedicated send and receive flags that trigger interrupts
- SPI bus busy flag;
- Hardware CRC for reliable communication;
  - In send mode, the CRC value can be sent as the last byte;
  - In full-duplex mode, CRC is automatically performed on the last byte received.
- Master mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffer with DMA capability: generates send and receive requests
- Maximum speed: SPI1 interface 36Mbps, SPI2/SPI3 interface 18Mbps

2.17 Serial audio interface (I^2S)

I^2S is a 3-pin synchronous serial interface communication protocol. The device integrates 2 standard I2S interfaces (multiplexed with SPI) and can operate in master or slave mode. I^2S can be configured for 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8KHz to 96KHz. It supports four audio standards, including Philips I^2S, MSB and LSB alignment, and PCM.

It can work in master and slave mode in half duplex communication. When it acts as a master device, it provides clock signals to external slave devices through an interface.

The main functions of I^2S interface are as follows;

- Simplex communication (send or receive only)
- Master or slave operations
- 8-bit linear programmable prescaler for accurate audio sampling frequencies (8 KHZ to 96KHz)
- The data format can be 16, 24, or 32 bits
- Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame)
- Programmable clock polarity (steady state)
- The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel
- Supported I^2S protocols:
  - I^2S Philips standard
  - MSB alignment standard (left aligned)
  - LSB alignment standard (right aligned)
  - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame)
- The data direction is always MSB first
- Both send and receive have DMA capability
- The master clock can be output to external audio devices at a fixed rate of 256xFs(Fs is the audio sampling frequency)

2.18 Quard serial peripheral interface (QSPI)

Integrated 1 channel QSPI single-host mode, can work in two modes of indirect and memory mapping.

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The main features of the QSPI controller are as follows:

- Can be configured as Single SPI/Dual SPI/Quard SPI mode. In Single mode, it supports standard SPI operation and can work in half-duplex and full-duplex modes
- The operation mode of SPI can be configured in indirect mode or memory mapping mode, the command code in the instruction stage can be configured, and the alternate byte or mode byte in the alternate byte stage or mode stage can be configured
- Support 8-bit, 16-bit, 32-bit data access mode
- Data transceiver FIFO
- Support DMA operation
- Support FIFO interrupt, operation completion interrupt, timeout interrupt, data access error interrupt
- Maximum speed supports 4×36Mbps
- In indirect mode or memory mapping mode, the operation is divided into instruction stage, address stage, alternate byte stage, Dummy stage, and data stage. These stages can be configured to be skipped.

2.19 Secure digital input output interface (SDIO)

Secure Digital Input and Output (Secure Digital Input and Output), referred to as SDIO interface, SDIO host interface provides an operation interface between AHB peripheral bus and Multimedia Card (MMC), SD memory card, SDIO card devices.

SDIO host functions are as follows:

- Support "MultiMediaCard System Specification Version 4.2", support 1-bit (default), 4-bit and 8-bit data bus, forward compatible with earlier MMC protocol
- Support "SD Memory Card Specifications Version 2.0"
- Support "SD I/O Card Specification Version 2.0", support 1-bit (default) and 4-bit data format
- SDIO clock rate up to 48MHz
- SDIO does not support SPI communication

2.20 Controller Area Network (CAN)

The device integrates 2 channel CAN bus interface compatible with 2.0A and 2.0B (active) specifications, with bit rates up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

Main features:

- Support CAN protocol 2.0A and 2.0B active mode
- Baud rate up to 1Mbps
- Supports time-triggered communication
- Send
  - 3 sending mailboxes
  - The priority of sent packets can be configured by software
  - Records the timestamp of the time when the SOF was sent
- Receive
  - Level 3 depth of 2 receiving FIFO
  - Variable filter group:
  - There are 14 filter groups
  - Identifier list

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- The FIFO overflow processing mode is configurable
- Record the time stamp of the receipt of the SOF

- Time-triggered communication mode
  - Disable automatic retransmission mode
  - 16-bit free run timer
  - Timestamp can be sent in the last 2 bytes of data
- Management
  - Interrupt masking
  - The mailbox occupies a separate address space to improve software efficiency

2.21 General purpose input and output interface (GPIO)

Up to 80 GPIO, which are divided into 5 groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE), each group has 16 ports. Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up/pull-down), or multiplexing peripheral function port. Most GPIO pins are shared with digital or analog multiplexing peripherals, and some I/O pins are multiplexed with clock pins. All GPIO pins except ports with analog input capability have high current passing capability.

The main features of GPIO are described as follows:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
  - Input floating
  - Input pull up (weak pull up)
  - Input pull down (weak pull down)
  - Analog input
  - Open drain output
  - Push-pull output
  - Push-pull multiplexing function
  - Open drain multiplexing function
- General I/O (GPIO)
  - During and just after reset, the alternate functions are not enabled, except for BOOT0 and BOOT1(BOOT0 and BOOT1 are input pull-down) and NRST pin, the I/O port is configured to analog input mode.
  - During and just after reset, the alternate function is not turned on, the I/O port is configured as analog input mode, and after reset, the JTAG pin is placed in input pull-up or pull-down mode:
    - ✓ JTDI in pull-up mode;
    - ✓ JTCK in drop down mode;
    - ✓ JTMS in pull-up mode;
    - ✓ NJTRST is placed in pull-up mode
  - When configured as output, values written to the output data registers are output to the appropriate I/O pins. Can be output in push pull mode or open drain mode
- Separate bit setting or bit clearing functions
- External interrupt/wake up: All ports have external interrupt capability. In order to use external interrupts, ports must be configured in input mode
- Alternate function: port bit configuration register must be programmed before using default alternate function

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- GPIO lock mechanism, which freezes I/O configurations. When a LOCK is performed on a port bit, the configuration of the port bit cannot be changed until the next reset

2.22 Analog/digital converter (ADC)

Up to 4 successive comparison ADC with 12-bit 4.7Msps sampling rate, support single-ended input and differential input, can measure 38 external and 7 internal signal sources. ADC1 support 9 external channels, ADC2 supports 12 external channels, ADC3 supports 15 external channels, ADC4 supports 13 external channels.

The main features of ADC are described as follows:

- Support 12/10/8/6-bit resolution configurable
  - The highest sampling rate at 12bit resolution is 4.7MSPS
  - The maximum sampling rate at 10bit resolution is 6.1MSPS
  - The maximum sampling rate at 8bit resolution is 7.3MSPS
  - The maximum sampling rate at 6bit resolution is 8.9MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - AHB_CLK can be configured as the working clock source, up to 144MHz
  - PLL can be configured as a sampling clock source, up to 80MHZ, support 1,2,4,6,8,10,12,16,32, 64,128,256 frequency division
  - AHB_CLK can be configured as the sampling clock source, up to 80MHz, and supports frequency 1,2,4,6,8,10,12,16,32
  - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Supports timer trigger ADC sampling
- Interrupts when conversion ends, injection conversion ends, and analog watchdog events occur
- Single and continuous conversion modes
- Automatic scan mode from channel 0 to channel N
- Support for self-calibration
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately by channel
- Both regular conversions and injection conversions have external triggering options
- Continuous mode
- Dual ADC mode, ADC1 and ADC2 combination, ADC3 and ADC4 combination
- ADC power supply requirements: 1.8V to 3.6V
- ADC input range: VREF- ≤ VIN ≤ VREF+
- ADC can use DMA operations, and DMA requests are generated during regular channel conversion.
- Analog watchdog function can monitor one, multiple, or all selected channels with great precision. When the monitored signal exceeds the preset threshold, an interruption will occur.

2.23 Digital-to-analog converter (DAC)

Support 2 digital-to-analog converters (DAC). DAC is a digital-to-analog converter with 12-bit digital input and voltage output. The DAC module has 2 output channels, each channel has a separate converter, and the 2 DAC can be used at the same time without affecting each other. The DAC can input the reference voltage VREF+ through the pin to obtain more accurate conversion results.

This dual digital interface supports the following functions:

- 2 DAC converters: each with an output channel

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- Configurable 8-bit or 12-bit output
- Configurable left and right data alignment in 12-bit mode
- Update function
- Generate noise wave
- Generate triangular wave
- Dual DAC channel independent or synchronous conversion
- Every channel can use DMA function.
- External trigger for conversion
- Input voltage VREF+

2.24 Operational amplifier (OPAMP)

Up to 4 independent operational amplifiers, with external amplification, internal follower and programmable amplifier (PGA) and other operating modes (or both internal amplification and external filtering).

The main functions are as follows:

- Support rail-to-rail input/output
- Can be configured as an independent op amp and programmable gain op amp
- Forward and reverse input check
- OPAMP working mode can be configured as:
  - Independent mode (external gain setting)
  - PGA mode, programmable gain set to 2X, 4X, 8X, 16X, 32X
  - Follower mode
- Internally connected ADC channel is used for output signal measurement of operational amplifier

2.25 Analog comparator (COMP)

The device integrates up to 7 comparators. It can be used as a separate device (all ports of the comparator are plugged into the I/O) or in combination with a timer. In the case of motor control, it can be combined with the PWM output from the timer to form periodic current control.

The main functions of comparator are as follows:

- Rail to rail comparators are supported
- The reverse and forward sides of the comparator support the following inputs
  - Optional I/O
  - DAC channel output
  - Internal adjustable voltage input (there are 2 internal adjustable voltages VREF1, VREF2, shared by all 7 comparators), 64-level uniform adjustment based on V_{DDA}
- Programmable hysteresis can be configured as no hysteresis, low hysteresis, medium hysteresis, and high hysteresis
- The comparator can output to EITHER I/O or timer input for triggering
  - Capture events
  - OCREF_CLR events (for periodic current control)
  - Brake events
- The comparator supports output filtering, including analog and digital filtering
- COMP1/COMP2, COMP3/COMP4 and COMP5/COMP6 can form a window comparator

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- Support comparator output with blanking, you can choose to disable blanking or choose Timer1_OC5/Timer8_OC5 as blanking input
- Each comparator can have interrupt wake up capability, support from SLEEP mode wake up

2.26 Temperature sensor (TS)

The temperature sensor produces a voltage that varies linearly with temperature in range of 1.8V < V_{DDA}< 3.6V. The temperature sensor is internally connected to the input channel of ADC1_IN16 for converting the output of the sensor to a digital value.

2.27 Cyclic redundancy check calculation unit (CRC)

Integrated CRC32 and CRC16 functions, the cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain any CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting flash memory errors, CRC cells can be used to calculate signatures of software in real time and compare them with signatures generated when linking and generating the software.

The CRC has the following features:

- CRC16: supports polynomials $X^{16} + X^{15} + X^2 + X^0$
- CRC32: supports polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- CRC16 calculation time: 1 AHB clock cycles (HCLK)
- CRC32 calculation time: 1 AHB clock cycles (HCLK)
- The initial value for cyclic redundancy computing is configurable
- Support DMA mode

2.28 Security Acceleration Engine (SAC)

Embedded algorithm hardware acceleration engine supports a variety of international algorithms and national cryptographic symmetric cryptographic algorithms and hash cryptographic algorithm acceleration, which can greatly improve the encryption and decryption speed compared with pure software algorithms.

The supported algorithms of hardware are as follows:

- Support DES symmetric algorithm
  - DES and 3DES encryption and decryption operations are supported
  - TDES supports 2KEY and 3KEY modes.
  - Support CBC and ECB modes
- AES symmetric algorithm is supported
  - 128bit/192bit/ 256bit key length is supported
  - Support CBC, ECB and CTR modes
- Support SHA hash algorithm
  - Support SHA1/SHA224/SHA256
- Support MD5 summarization algorithm
- Support symmetric national secret SM1, SM4, SM7 algorithm and SM3 hash algorithm.

2.29 Unique device serial number (UID)

N32A455xxL7 series products have two built-in unique device serial numbers of different lengths, which are 96-bit Unique Device ID (UID) and 128-bit Unique Customer ID (UCID). These two device serial numbers are stored in the system configuration block of flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32A455xxL7 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

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The 96-bit UID is usually used as a serial number or password. When writing flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in flash memory.

UCID is 128-bit, which complies with the definition of national technology chip serial number. It contains the information related to chip production and version.

2.30 Serial single-wire JTAG debug port (SWJ-DP)

Embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-line debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

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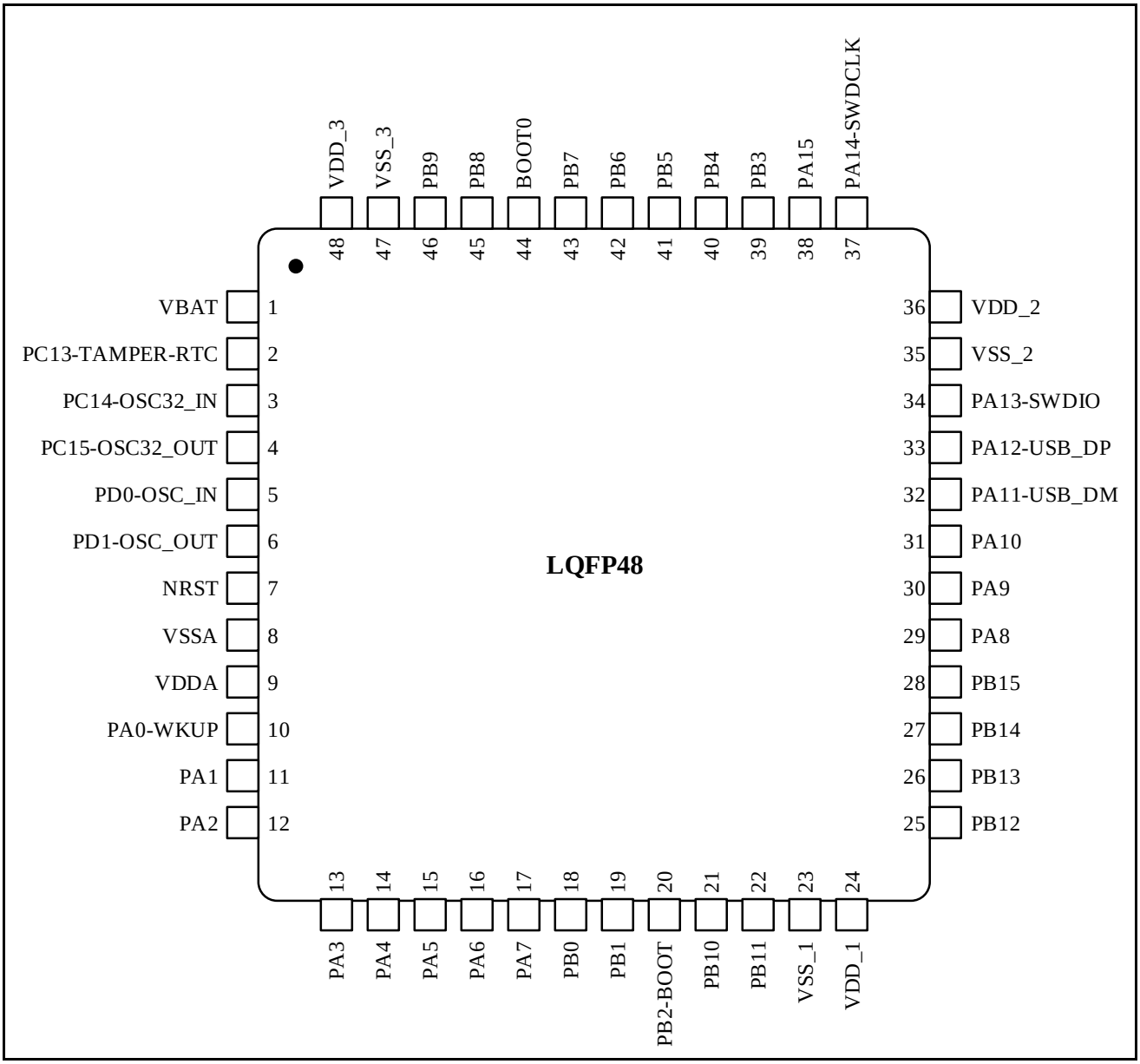
3 Pinouts and description

3.1 Pinouts

3.1.1 LQFP48

Figure 3-1 N32A455xxL7 Series LQFP48 pinout



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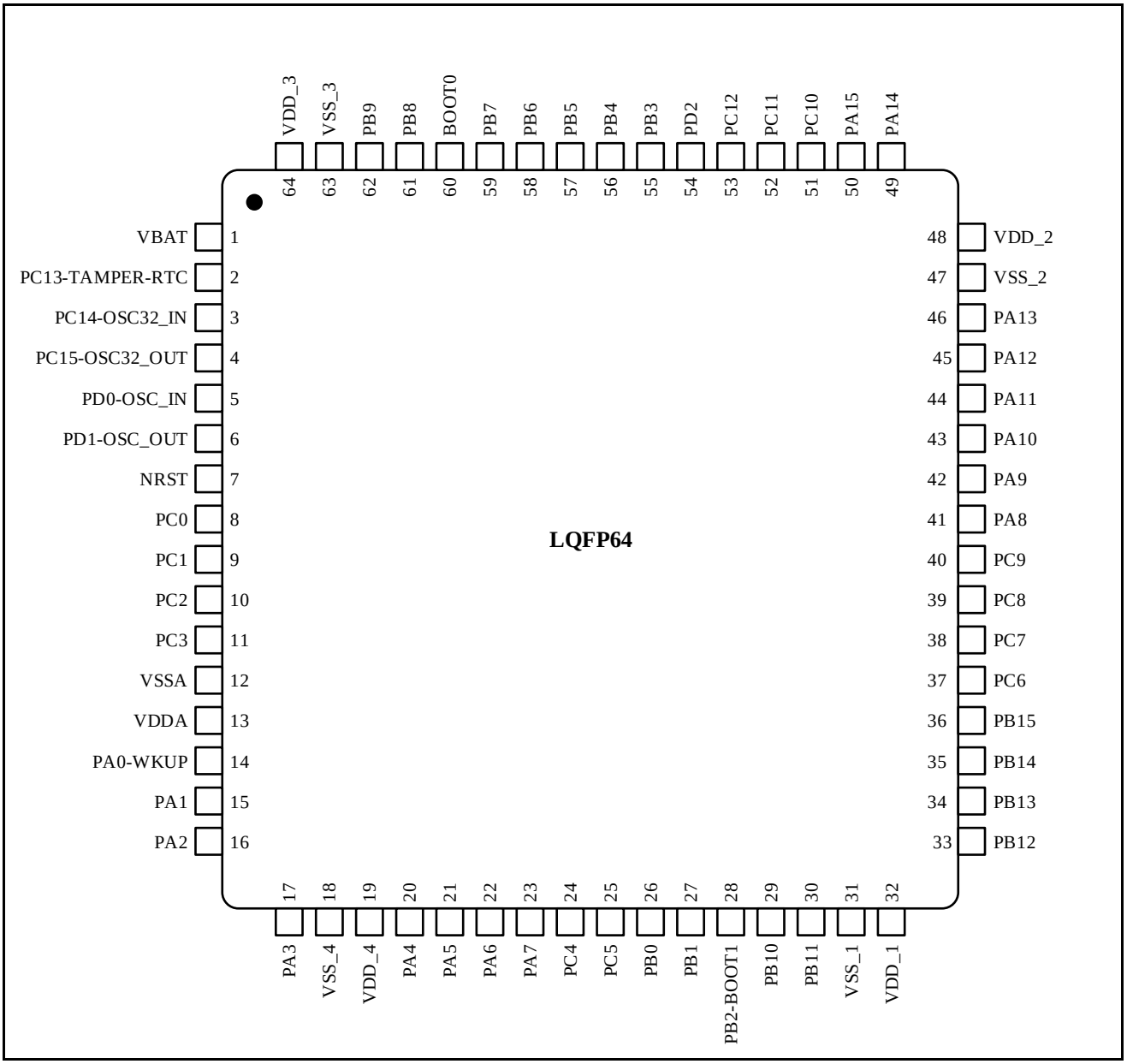
3.1.2 LQFP64

Figure 3-2 N32A455xxL7 Series LQFP64 pinout



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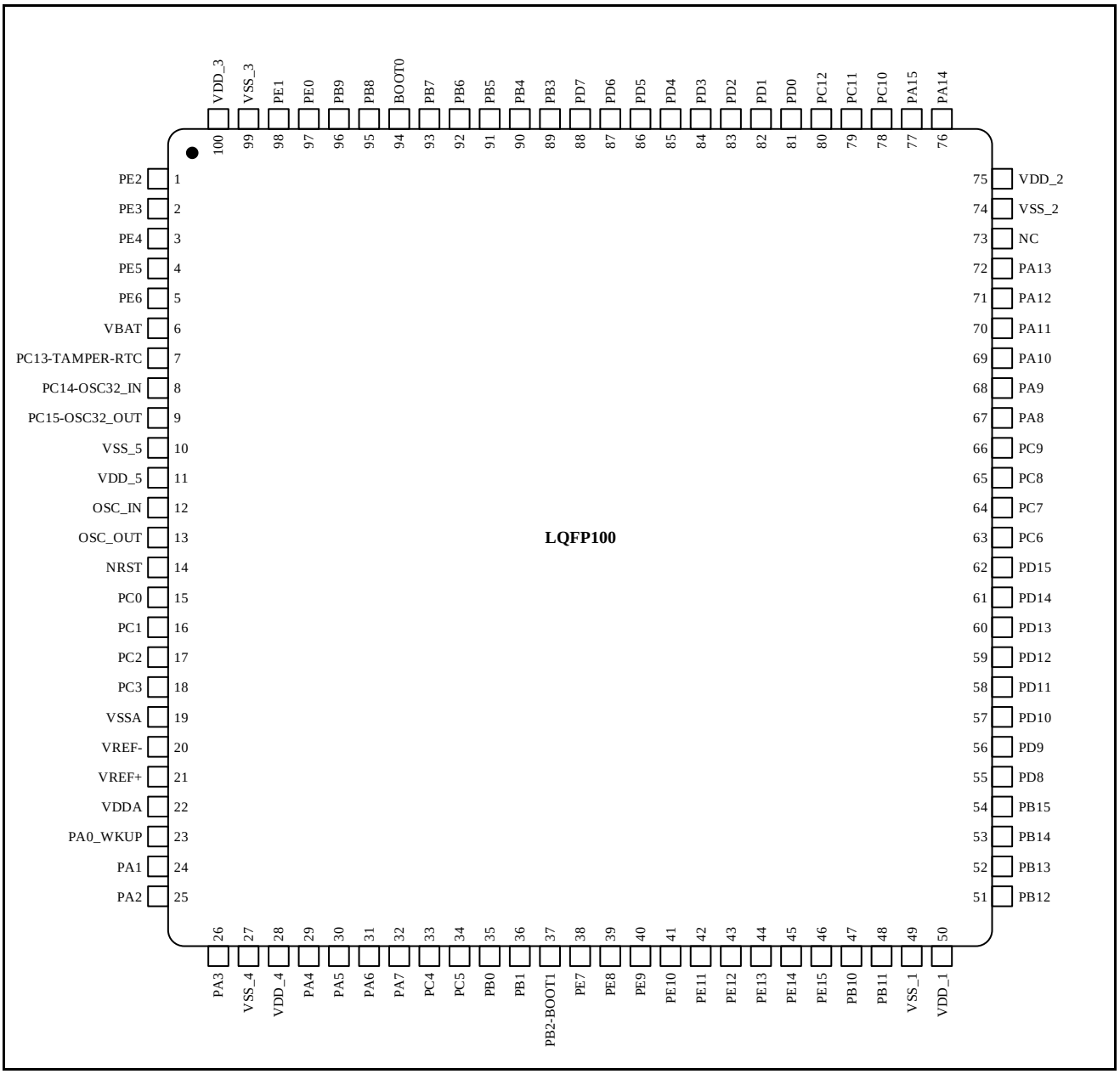
3.1.3 LQFP100

Figure 3-3 N32A455xxL7 Series LQFP100 pinout



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3.2 Pin definition

For details of alternate functions for IO, please refer to the "Alternate function" section within the "GPIO and AFIO" chapter of the User Manual.

Table 3-1 Pin definition

Package			Pin name	Type (1)	I / O structure(2)	Fail-safe support(8)	Main functions(3) (after reset)	Optional multiplexing function(6)	
LQFP48	LQFP64	LQFP100						Default	Redefine
-	-	1	PE2	I/O	FT	Yes	PE2	UART6_TX	-
-	-	2	PE3	I/O	FT	Yes	PE3	UART6_RX	-
-	-	3	PE4	I/O	FT	Yes	PE4	-	-
-	-	4	PE5	I/O	FT	Yes	PE5	-	-
-	-	5	PE6	I/O	FT	Yes	PE6	-	-
1	1	6	VBAT	S	-	-	VBAT	-	-
2	2	7	PC13-TAMPER- RTC(4)	I/O	TC	Yes	PC13(5)	TAMPER-RTC	-
3	3	8	PC14- OSC32_IN(4)	I/O	TC	Yes	PC14(5)	OSC32_IN	-
4	4	9	PC15- OSC32_OUT(4)	I/O	TC	Yes	PC15(5)	OSC32_OUT	-
-	-	10	VSS_5	S	-	-	VSS_5	-	-
-	-	11	VDD_5	S	-	-	VDD_5	-	-
5	5	12	OSC_IN(7)	I	TC	Yes	OSC_IN	-	-
6	6	13	OSC_OUT(7)	O	TC	No	OSC_OUT	-	-
7	7	14	NRST	I/O	-	-	NRST	-	-
-	8	15	PC0	I/O	TTa	No	PC0	ADC12_IN6(10) I2C3_SCL	COMP7_INM UART6_TX
-	9	16	PC1	I/O	TTa	No	PC1	ADC12_IN7(10) I2C3_SDA	COMP7_INP UART6_RX
-	10	17	PC2	I/O	TTa	No	PC2	ADC12_IN8(10) COMP7_OUT	UART7_TX SPI3_NSS I2S3_WS
-	11	18	PC3	I/O	TTa	No	PC3	ADC12_IN9(10)	UART7_RX SPI3_SCK I2S3_CK OPAMP3_VINP OPAMP4_VINP COMP5_INP
8	12	19	VSSA	S	-	-	VSSA	-	-
		20	VREF-	S	-	-	VREF-	-	-
9	13	21	VREF+	S	-	-	VREF+	-	-
		22	VDDA	S	-	-	VDDA	-	-
10	14	23	PA0-WKUP	I/O	TTa	No	PA0	WKUP USART2_CTS ADC1_IN1(9) TIM2_CH1_ETR TIM5_CH1 TIM8_ETR COMP1_OUT	COMP1_INM SPI3_MISO
11	15	24	PA1	I/O	TTa	No	PA1	USART2_RTS ADC1_IN2(9) TIM5_CH2 TIM2_CH2	COMP1_INP OPAMP1_VINP OPAMP3_VINP SPI3_MOSI I2S3_SD
12	16	25	PA2	I/O	TTa	No	PA2	USART2_TX	OPAMP1_VINM

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Package			Pin name	Type [1]	I / O structure[2]	Fail-safe support[8]	Main functions[3] (after reset)	Optional multiplexing function[6]	
LQFP48	LQFP64	LQFP100						Default	Redefine
								TIM5_CH3 ADC12_IN11[10] TIM2_CH3 COMP2_OUT	OPAMP2_VINM
13	17	26	PA3	I/O	TTa	No	PA3	USART2_RX TIM5_CH4 ADC1_IN4[9] TIM2_CH4	OPAMP1_VINM OPAMP1_VINP COMP5_INP
-	18	27	VSS_4	S	-	-	VSS_4	-	-
-	19	28	VDD_4	S	-	-	VDD_4	-	-
14	20	29	PA4	I/O	TTa	No	PA4	SPI1_NSS USART2_CK DAC_OUT1 ADC2_IN1[9] QSPI_NSS	COMP1_INM COMP2_INM COMP3_INM COMP4_INM COMP5_INM COMP6_INM COMP7_INM OPAMP4_VINP I2C2_SCL
15	21	30	PA5	I/O	TTa	No	PA5	SPI1_SCK DAC_OUT2 ADC2_IN2[9] QSPI_SCK	COMP1_INM COMP2_INM COMP3_INM COMP4_INM COMP5_INM COMP6_INM COMP7_INM OPAMP1_VINP OPAMP2_VINM OPAMP3_VINP I2C2_SDA
16	22	31	PA6	I/O	TTa	No	PA6	SPI1_MISO TIM8_BKIN ADC1_IN3[9] TIM3_CH1 QSPI_IO0	TIM1_BKIN OPAMP1_VOUT COMP2_OUT
17	23	32	PA7	I/O	TTa	No	PA7	SPI1_MOSI TIM8_CH1N ADC2_IN4[9] TIM3_CH2 QSPI_IO1 COMP2_OUT	TIM1_CH1N COMP2_INP OPAMP1_VINP OPAMP2_VINP COMP6_INM
-	24	33	PC4	I/O	TTa	No	PC4	ADC2_IN5[9] QSPI_IO2 UART7_TX	I2C3_SCL OPAMP3_VINM COMP4_INM COMP5_INP
-	25	34	PC5	I/O	TTa	No	PC5	ADC2_IN12[10] QSPI_IO3 UART7_RX	I2C3_SDA OPAMP4_VINP COMP4_OUT COMP6_INP
18	26	35	PB0	I/O	TTa	No	PB0	ADC3_IN12[10] TIM3_CH3 TIM8_CH2N	TIM1_CH2N UART6_TX OPAMP2_VINP COMP3_INP COMP5_OUT

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Package			Pin name	Type (1)	I / O structure(2)	Fail-safe support(8)	Main functions(3) (after reset)	Optional multiplexing function(6)	
LQFP48	LQFP64	LQFP100						Default	Redefine
19	27	36	PB1	I/O	TTa	No	PB1	ADC2_IN3(9) TIM3_CH4 TIM8_CH3N COMP4_OUT	TIM1_CH3N OPAMP2_VOUT UART6_RX COMP2_INM COMP1_OUT
20	28	37	PB2	I/O	TTa	No	PB2/BOOT1	ADC2_IN13(10)	UART4_TX SPI1_NSS
-	-	38	PE7	I/O	TTa	No	PE7	ADC3_IN13(10)	TIM1_ETR UART4_RX SPI1_SCK COMP3_INM
-	-	39	PE8	I/O	TTa	No	PE8	ADC34_IN6(10)	TIM1_CH1N UART5_TX SDIO_DAT0 SPI1_MISO OPAMP2_VINP COMP2_INM
-	-	40	PE9	I/O	TTa	No	PE9	ADC3_IN2(9)	TIM1_CH1 UART5_RX SDIO_DAT1 SPI1_MOSI
-	-	41	PE10	I/O	TTa	No	PE10	ADC3_IN14(10)	TIM1_CH2N SDIO_DAT2 SPI2_NSS I2S2_WS
-	-	42	PE11	I/O	TTa	No	PE11	ADC3_IN15(10)	TIM1_CH2 SDIO_DAT3 SPI2_SCK I2S2_CK
-	-	43	PE12	I/O	TTa	No	PE12	ADC3_IN4(9)	TIM1_CH3N SDIO_CLK SPI2_MISO
-	-	44	PE13	I/O	TTa	No	PE13	ADC3_IN3(9)	TIM1_CH3 SPI2_MOSI I2S2_SD SDIO_CMD
-	-	45	PE14	I/O	TTa	No	PE14	ADC4_IN1(9)	TIM1_CH4
-	-	46	PE15	I/O	TTa	No	PE15	ADC4_IN2(9)	TIM1_BKIN
21	29	47	PB10	I/O	TTa	Yes	PB10	I2C2_SCL USART3_TX	TIM2_CH3 COMP5_INM OPAMP3_VINM OPAMP4_VINM COMP1_INP COMP3_OUT
22	30	48	PB11	I/O	TTa	No	PB11	I2C2_SDA USART3_RX ADC3_IN1(9)	TIM2_CH4 OPAMP3_VOUT COMP2_INP COMP5_OUT
23	31	49	VSS_1	S	-	-	VSS_1	-	-
24	32	50	VDD_1	S	-	-	VDD_1	-	-

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Package			Pin name	Type (1)	I / O structure(2)	Fail-safe support(8)	Main functions(3) (after reset)	Optional multiplexing function(6)	
LQFP48	LQFP64	LQFP100						Default	Redefine
25	33	51	PB12	I/O	TTa	No	PB12	SPI2_NSS I2S2_WS I2C2_SMBA USART3_CK TIM1_BKIN CAN2_RX ADC4_IN3(9)	COMP3_INM OPAMP4_VOUT COMP4_OUT
26	34	52	PB13	I/O	TTa	No	PB13	SPI2_SCK I2S2_CK USART3_CTS TIM1_CH1N CAN2_TX ADC3_IN5(9)	UART5_TX COMP4_INM
27	35	53	PB14	I/O	TTa	No	PB14	SPI2_MISO TIM1_CH2N USART3_RTS ADC4_IN4(9)	COMP3_INP UART5_RX
28	36	54	PB15	I/O	TTa	No	PB15	SPI2_MOSI I2S2_SD TIM1_CH3N ADC4_IN5(9)	COMP4_INP
-	-	55	PD8	I/O	TTa	No	PD8	ADC4_IN12(10)	USART3_TX OPAMP4_VINM SPI3_NSS I2S3_WS CAN1_RX COMP6_INM
-	-	56	PD9	I/O	TTa	No	PD9	ADC4_IN13(10)	USART3_RX SPI3_SCK I2S3_CK CAN1_TX COMP6_INP
-	-	57	PD10	I/O	TTa	No	PD10	ADC34_IN7(10)	USART3_CK CAN2_RX COMP5_INM
-	-	58	PD11	I/O	TTa	No	PD11	ADC34_IN8(10)	USART3_CTS CAN2_TX SPI3_MISO
-	-	59	PD12	I/O	TTa	No	PD12	ADC34_IN9(10)	TIM4_CH1 USART3_RTS SPI3_MOSI I2S3_SD COMP7_OUT
-	-	60	PD13	I/O	TTa	No	PD13	ADC34_IN10(10)	TIM4_CH2
-	-	61	PD14	I/O	TTa	No	PD14	ADC34_IN11(10)	TIM4_CH3 I2C4_SCL TIM8_CH1
-	-	62	PD15	I/O	FT	Yes	PD15	-	TIM4_CH4 I2C4_SDA TIM8_CH2
-	37	63	PC6	I/O	TC	Yes	PC6	I2S2_MCK TIM8_CH1 SDIO_DAT6 I2C4_SCL	TIM3_CH1 SPI2_NSS I2S2_WS USART2_CTS
-	38	64	PC7	I/O	TC	Yes	PC7	I2S3_MCK	TIM3_CH2

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Package			Pin name	Type (1)	I / O structure(2)	Fail-safe support(8)	Main functions(3) (after reset)	Optional multiplexing function(6)	
LQFP48	LQFP64	LQFP100						Default	Redefine
								TIM8_CH2 SDIO_DAT7 I2C4_SDA	SPI2_SCK I2S2_CK USART2_RTS
-	39	65	PC8	I/O	TC	Yes	PC8	TIM8_CH3 SDIO_DAT0	TIM3_CH3 SPI2_MISO USART2_TX
-	40	66	PC9	I/O	TTa	Yes	PC9	TIM8_CH4 SDIO_DAT1	TIM3_CH4 SPI2_MOSI I2S2_SD USART2_RX COMP6_OUT OPAMP3_VINP OPAMP4_VINM COMP4_INP
29	41	67	PA8	I/O	FT	Yes	PA8	USART1_CK TIM1_CH1 MCO	-
30	42	68	PA9	I/O	FT	Yes	PA9	USART1_TX TIM1_CH2	I2C4_SCL
31	43	69	PA10	I/O	FT	Yes	PA10	USART1_RX TIM1_CH3	I2C4_SDA
32	44	70	PA11	I/O	FT	Yes	PA11	USART1_CTS USBDM CAN1_RX TIM1_CH4 COMP1_OUT	COMP5_OUT
33	45	71	PA12	I/O	FT	Yes	PA12	USART1_RTS USBDP CAN1_TX TIM1_ETR COMP2_OUT	COMP6_OUT
34	46	72	PA13	I/O	FT	Yes	JTMS- SWDIO	-	PA13 UART4_TX
-	-	73	Not Connect						
35	47	74	VSS_2	S	-	-	VSS_2	-	-
36	48	75	VDD_2	S	-	-	VDD_2	-	-
37	49	76	PA14	I/O	FT	Yes	JTCK- SWCLK	-	PA14 UART4_RX
38	50	77	PA15	I/O	FT	Yes	JTDI	SPI3_NSS I2S3_WS	TIM2_CH1_ETR PA15 SPI1_NSS USART2_CTS TIM8_CH1N

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Package			Pin name	Type (1)	I / O structure(2)	Fail-safe support(8)	Main functions(3) (after reset)	Optional multiplexing function(6)	
LQFP48	LQFP64	LQFP100						Default	Redefine
-	51	78	PC10	I/O	TTa	Yes	PC10	UART4_TX SDIO_DAT2	USART3_TX SPI3_SCK I2S3_CK QSPI_NSS COMP3_OUT
-	52	79	PC11	I/O	TTa	Yes	PC11	UART4_RX SDIO_DAT3	USART3_RX SPI3_MISO QSPI_SCK COMP4_OUT
-	53	80	PC12	I/O	TC	Yes	PC12	UART5_TX SDIO_CLK	USART3_CK SPI3_MOSI I2S3_SD QSPI_IO0 TIM8_CH2N
-	-	81	PD0	I/O	FT	Yes	PD0(7)	-	CAN1_RX UART4_TX QSPI_IO1
-	-	82	PD1	I/O	FT	Yes	PD1(7)	-	CAN1_TX UART4_RX QSPI_IO2
-	54	83	PD2	I/O	TC	Yes	PD2	TIM3_ETR UART5_RX SDIO_CMD	SPI3_NSS I2S3_WS QSPI_IO3 TIM8_CH3N
-	-	84	PD3	I/O	FT	Yes	PD3	-	USART2_CTS
-	-	85	PD4	I/O	TC	Yes	PD4	-	USART2_RTS
-	-	86	PD5	I/O	TC	Yes	PD5	-	USART2_TX
-	-	87	PD6	I/O	TC	Yes	PD6	-	USART2_RX
-	-	88	PD7	I/O	TC	Yes	PD7	-	USART2_CK
39	55	89	PB3	I/O	FT	Yes	JTDO	SPI3_SCK I2S3_CK	PB3 TRACESWO TIM2_CH2 SPI1_SCK USART2_RTS TIM8_BKIN
40	56	90	PB4	I/O	FT	Yes	NJTRST	SPI3_MISO	PB4 TIM3_CH1 SPI1_MISO USART2_TX TIM8_ETR
41	57	91	PB5	I/O	FT	Yes	PB5	I2C1_SMBA SPI3_MOSI I2S3_SD	TIM3_CH2 SPI1_MOSI CAN2_RX USART2_RX TIM1_BKIN
42	58	92	PB6	I/O	TTa	Yes	PB6	I2C1_SCL TIM4_CH1	USART1_TX CAN2_TX COMP5_OUT

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Package			Pin name	Type [1]	I / O structure[2]	Fail-safe support[8]	Main functions[3] (after reset)	Optional multiplexing function[6]	
LQFP48	LQFP64	LQFP100						Default	Redefine
43	59	93	PB7	I/O	TTa	Yes	PB7	I2C1_SDA TIM4_CH2	USART1_RX COMP6_OUT
44	60	94	BOOT0	I	-	-	BOOT0	-	-
45	61	95	PB8	I/O	TTa	Yes	PB8	TIM4_CH3 SDIO_DAT4 COMP1_OUT	I2C1_SCL CAN1_RX UART5_TX
46	62	96	PB9	I/O	TTa	Yes	PB9	TIM4_CH4 SDIO_DAT5 COMP2_OUT	I2C1_SDA CAN1_TX UART5_RX
-	-	97	PE0	I/O	FT	Yes	PE0	TIM4_ETR	-
-	-	98	PE1	I/O	FT	Yes	PE1	-	-
47	63	99	VSS_3	S	-	-	VSS_3	-	-
48	64	100	VDD_3	S	-	-	VDD_3	-	-

1. *I = input, O = output, S = power supply, HiZ = high impedance.*
2. *FT: tolerate 5V; TTa: tolerates 3.3V and supports analog peripherals; TC: ordinary 3.3V I/O*
3. *Some functions are only supported in some models of chips.*
4. *Pin PC13, PC14 and PC15 are powered by the power switch, which can only absorb limited current (3mA). Therefore, when these three pins are used as output pins, they have the following limitations: only one pin can be used as output at the same time; when they are used as output pins, they can only work in 2MHz mode, and the maximum driving load is 30pF, and they cannot be used as current sources (such as driving LEDs).*
5. *When the backup area is powered on for the first time, these pins are in the main function state. After that, even if they are reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these IO ports, please refer to the battery backup area of N32A455 user's reference manual and relevant chapters of BKP register.*
6. *Some multiplexing functions can be configured to other pins by software (if the corresponding package model has this pin). For details, please refer to the multiplexing function I/O chapter and debugging setting chapter of N32A455 user reference manual.*
7. *Pin 5 and pin 6 of LQFP48/64 package are configured as OSC_IN and OSC_OUT function pins by default after the chip is reset. Software can reset these two pins to PD0 and PD1 functions. When used as PD0 and PD1, these two pins can only be used as ordinary IO functions. However, for LQFP100 package, because PD0 and PD1 are inherent functional pins, there is no need to re-image by software. For more details, please refer to the reuse function I/O chapter and debugging settings chapter of N32A455 user reference manual.*
8. *Fail-safe means that when the chip has no power input, the input high level is added to IO, and there is no phenomenon that the input high level is poured into the chip, which leads to a certain voltage on the power supply and consumes current.*
9. *Corresponding ADC channels are fast channels, support the highest sampling rate 4.7MSPS (12 bit)*
10. *Corresponding ADC channels are slow channels, support the highest sampling rate 4.7MSPS (12 bit)*

Note: ADC12_INx appears in the pin name label in the Table, indicating that this pin can be ADC1_INx or ADC2_INx. For example, ADC12_IN9 indicates that this pin can be configured as ADC1_IN9 or ADC2_IN9.

Similarly, ADC34_INx appears in the pin name annotation in the Table, indicating that this pin can be ADC3_INx or ADC4_INx.

TIM2_CH1_ETR in the multiplexing function corresponding to pin PA0 in the Table indicates that the function can be configured as TIM2_CH1 or TIM2_ETR. Similarly, the name of the remapping multiplexing function corresponding to PA15, TIM2_CH1_ETR, has the same meaning.

For the port of FT in the Table, it is necessary to ensure that the difference between IO voltage and power supply voltage is less than 3.6V

11. *VDDA/VSSA pins do not allow floating*

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4 Electrical specification

4.1 Parameter condition

All voltages are based on VSS unless otherwise specified.

4.1.1 Minimum and maximum values

Unless otherwise specified, all product are tests at ambient temperatures T_A=25 ℃.where minimums and maximums values apply to the worst ambient temperature, supply voltage and clock frequency specified in the datasheet.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production; Base on comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean ±3∑).

4.1.2 Typical numerical value

Unless otherwise specified, typical data are based on T_A= 25 C and V_{DD}=3.3V. These data is untested and used only as a design guide for the user.

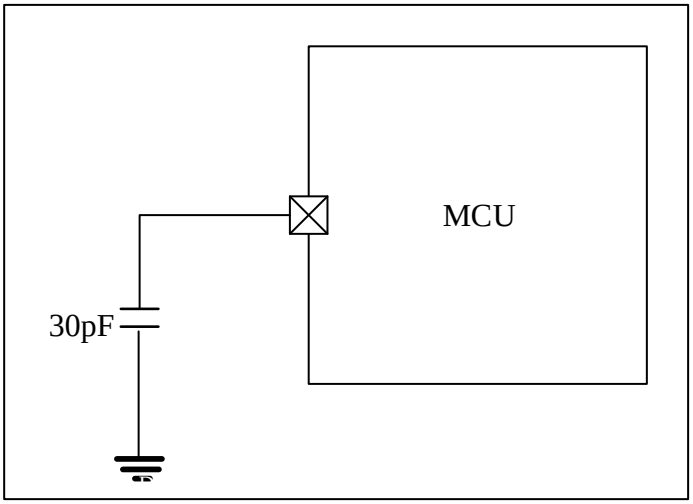
4.1.3 Typical curve

Unless otherwise specified, these typical curves are untested and used only as a design guide for the user.

4.1.4 Loading capacitor

The load conditions for measuring pin parameters are shown in Figure 4-1.

Figure 4-1 Pin load conditions



4.1.5 Pin input voltage

The measurement of the input voltage on pin is shown in Figure 4-2.

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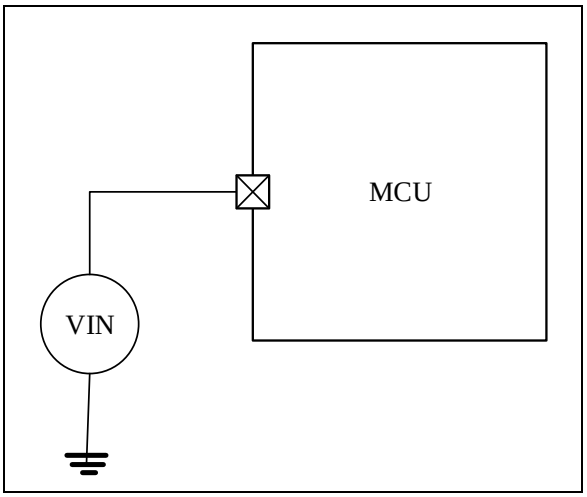
Figure 4-2 Pin voltage



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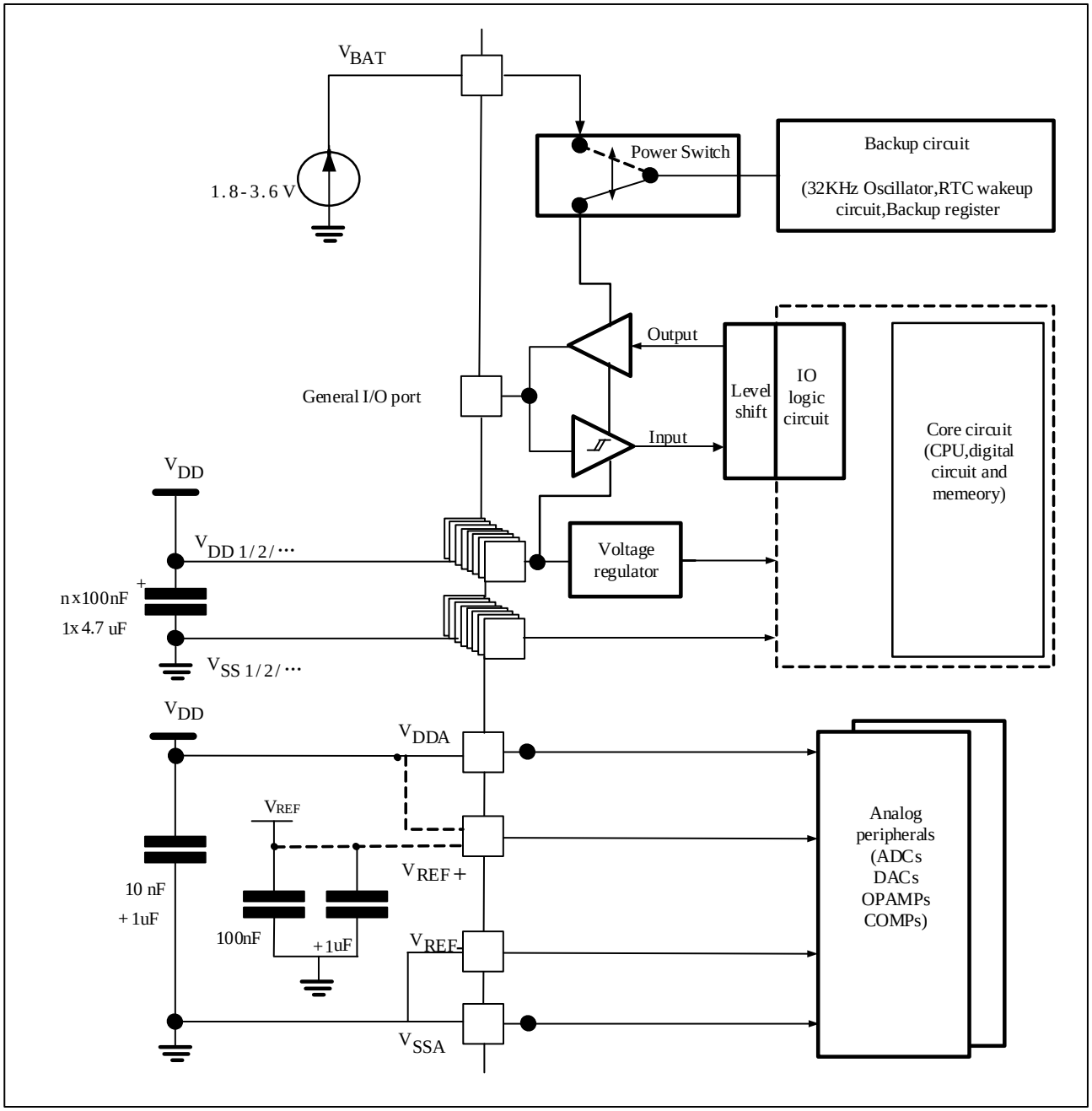
4.1.6 Power supply scheme

Figure 4-3 Power supply scheme



Note: The 4.7μF capacitor in the above figure must be connected to V_{DD3}.

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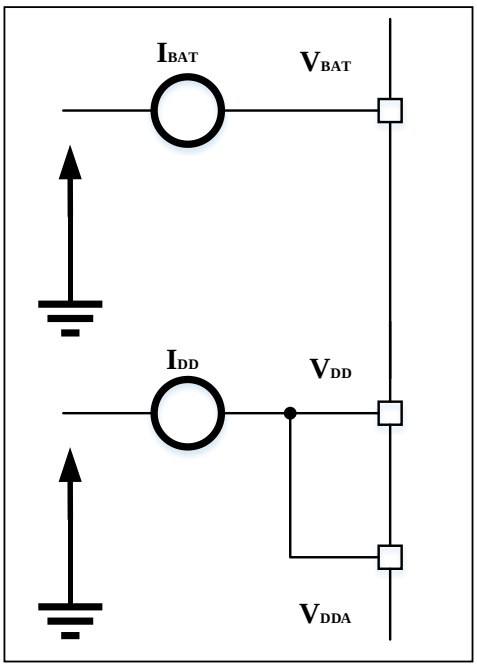
4.1.7 Current consumption measurement

Figure 4-4 Current consumption measurement scheme



4.2 Absolute maximum rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1、Table 4-2). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage characteristic

Symbol	Describe	Min	Max	Unit
V_{DD}- V_{SS}	Main power supply voltage (including V_{DDA} and V_{DD})(1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS}-0.3	5.5	
	Input voltage on other pins(2)	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different supply pins	-	50	mV
$\lvert V_{SSx}$- $V_{SS} \rvert$	Voltage difference between different grounding pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body mode)	See paragraph 4.3.11 festival		

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.
2. V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.
3. When 5.5V is applied to the 5V tolerant pin, V_{DD} cannot be less than 2.25V.

Table 4-2 Current characteristic

Symbol	Describe	Max(1)	Unit
I_{VDD}	Total current (supply current) through V_{DD}/V_{DDA} power line(1)(4)	100	mA
I_{VSS}	Total current (outflow current) through V_{SS} ground wire	100	
I_I	Output sink current on any I/O and control pins	12	
	Output current on any I/O and control pins	-12	
$I_{INJ(PIN)}$(2)(3)	Injection current of NRST pin	-5/0	
	Injection current of other pins(4)	+/-5	

1. All the power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA})pins of must always be connected to the power supply system within the external allowable range.

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2. When $V_{IN}>V_{DD}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current. $I_{INJ(PIN)}$ should not exceed its maximum value. Voltage characteristics refer to Table 4-1.
3. Reverse injection current can interfere with the analog performance of the device. See section 4.3.20.
4. When the maximum current occurs, the maximum allowable voltage drop of V_{DD} is $0.1V_{DD}$.

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-3 General working conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	144	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard working voltage	-	1.8	3.6	V
V_{DDA}	Analog working voltage	Must be the same as V_{DD}(1)	1.8	3.6	V
V_{BAT}	Backup partial working voltage	-	1.8	3.6	V
T_A	Ambient temperature	Maximum power consumption	-40	105	℃
T_J	Junction temperature range	-	-40	125	℃

1. It is recommended that the same power supply be used to power the V_{DD} and V_{DDA}. During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA}.

4.3.2 Operating conditions at power-on and power-off

Table 4-4 Operating conditions at power-on and power-off

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rising rate	Supply voltage goes from 0 to V_{DD}	20	-	μs/V
	V_{DD} falling rate	Supply voltage drops from V_{DD} to 0	80	-	

4.3.3 Embedded reset and power control module features

Table 4-5 Features of embedded reset and power control modules

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Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detector (MSB of PWR_CTRL is 0)	PRS[2:0]=000 (rising edge)	2.09	2.18	2.27	V
		PRS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PRS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PRS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PRS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PRS[2:0]=010 (falling edge)	2.19	2.28	2.37	V
		PRS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PRS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PRS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PRS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PRS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PRS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PRS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PRS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PRS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PRS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
	Level selection of programmable voltage detector (MSB of PWR_CTRL is 1)	PRS[2:0]=000 (rising edge)	1.7	1.78	1.85	V
		PRS[2:0]=000 (falling edge)	1.61	1.68	1.75	V
		PRS[2:0]=001 (rising edge)	1.8	1.88	1.96	V
		PRS[2:0]=001 (falling edge)	1.7	1.78	1.85	V
		PRS[2:0]=010 (rising edge)	1.9	1.98	2.06	V
		PRS[2:0]=010 (falling edge)	1.8	1.88	1.96	V
		PRS[2:0]=011 (rising edge)	2	2.08	2.16	V
		PRS[2:0]=011 (falling edge)	1.9	1.98	2.06	V
		PRS[2:0]=100 (rising edge)	3.15	3.28	3.41	V
		PRS[2:0]=100 (falling edge)	3.05	3.18	3.31	V
		PRS[2:0]=101 (rising edge)	3.24	3.38	3.52	V
		PRS[2:0]=101 (falling edge)	3.15	3.28	3.41	V
		PRS[2:0]=110 (rising edge)	3.34	3.48	3.62	V
		PRS[2:0]=110 (falling edge)	3.24	3.38	3.52	V
		PRS[2:0]=111 (rising edge)	3.44	3.58	3.72	V
		PRS[2:0]=111 (falling edge)	3.34	3.48	3.62	V
$V_{PVD\ hyst}$(1)	PVD hysteresis	-	-	100	-	mV
V_{POR}	VDD power-on/power-off reset threshold	-	-	1.64/1.62	-	V
$T_{RSTTEMPO}$(1)	Reset duration	-	-	0.8	4	ms

1. Guaranteed by design, not tested in production.

4.3.4 Embedded reference voltage

The parameters given in the following table are based on the ambient temperature and VDD supply voltage listed in Table 4-3.

Table 4-6 Embedded reference voltage

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Built-in reference voltage	-40 ℃< T_A< +85 ℃	1.16	1.20	1.24	V
		-40℃< T_A< +105℃	1.16	1.20	1.26	V
$T_{S\_vrefint}$(1)	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1(2)	µs

1. The shortest sampling time is obtained through multiple cycles in the application.
2. Guaranteed by design, not tested in production.

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4.3.5 Power supply current characteristics

Current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, I/O pin flip rate, program location in memory, and code executed.

The measurement method of current consumption is described in Figure 4-4.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum current consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- VDD or VSS (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting periods when 0 < SYSCLK ≤ 32 MHz; 1 waiting periods when 32 MHz < SYSCLK ≤ 64 MHz; 2 waiting periods when 64 MHz < SYSCLK ≤ 96 MHz; 3 waiting periods when 96 MHz < SYSCLK ≤ 128 MHz; 4 waiting periods when 128 MHz < SYSCLK ≤ 144 MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$.

The parameters given in Table 4-7 and Table 4-8 are based on the test at ambient temperature and V_{DD} supply voltage listed in Table 4-3.

Table 4-7 Maximum current consumption in run mode with data processing code running from internal flash memory

Symbol	Parameter	Condition	f_{HCLK}	Typ (1) T_A = 105°C	Unit
I_{DD}	Supply current in operation mode	External clock(2), Enable all peripherals	144MHz	32	mA
			72MHz	18	
			36MHz	11	
		External clock(2), Turn off all peripherals.	144MHz	15.8	
			72MHz	9.7	
			36MHz	7	

1. Based on comprehensive evaluation, not tested in production.
2. PLL is enabled when f_{HCLK}>8MHz.

Table 4-8 Maximum current consumption in sleep mode

Symbol	Parameter	Condition	f_{HCLK}	Typ (1) T_A = 105°C	Unit
I_{DD}	Supply current in sleep mode	External clock(2), Enable all peripherals	144MHz	27	mA
			72MHz	15.5	
			36MHz	10	
		External clock(2), Turn off all peripherals.	144MHz	9.4	
			72MHz	6.8	
			36MHz	5.5	

1. Based on comprehensive evaluation, not tested in production.
2. PLL is enabled when f_{HCLK}>8MHz.

4.3.5.2 Low power mode current consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- VDD or VSS (no load).
- All peripherals are disabled unless otherwise noted.

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Table 4-9 Typical and maximum current consumption in powerdown mode and standby mode

Symbol	Parameter	Condition	Typ (1)		Unit
			T_A =25 ℃	T_A =105 ℃	
I_{DD}	Supply current in STOP0 mode	The voltage regulator is in operation mode, low-speed and high-speed internal RC oscillators and high-speed oscillators are off (Independent watchdog is off)	300	4500	μA
		The voltage regulator is in low power consumption mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off (Independent watchdog is off)	150	3500	
	Supply current in STOP2 mode	The external low-speed clock is turned on, RTC is running, R-SRAM is maintained, all I/O states are maintained, and the independent watchdog is off.	10	300	
	Supply current in STANDBY mode	Low-speed RC oscillator and independent watchdog are on.	4	200	
		The internal low-speed RC oscillator is on, and the independent watchdog is off.	3.9	185	
		The internal low-speed RC oscillator and independent watchdog are off, and the low-speed oscillator and RTC is off.	3.7	155	
I_{DD_VBAT}	Supply current of Backup Area (VBAT)	Low speed oscillator and RTC is on.	3	20	

1. Typical values are measured at V_{DD}/V_{BAT} = 3.3v
2. Based on comprehensive evaluation, not tested in production.

4.3.5.3 Typical current consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- VDD or VSS (no load).
- All peripherals are disabled unless otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 96MHz, 3 waiting periods from 96MHz to 128MHz, 4 waiting periods from 128MHz to 144MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 4-3.
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$.

Table 4-10 Typical current consumption in running mode, data processing code runs from internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Typ (1)		Unit
				Enable all peripherals(2)	Disable all peripherals.	
I_{DD}	Supply current in operation mode	External clock(3)	144MHz	30.3	14.2	mA
			72MHz	17	8.1	
			36MHz	9.3	5.3	
		Run in high-speed internal RC oscillator (HSI), use AHB prescaler to reduce frequency.	128MHz	30	12.7	mA
			72MHz	22.5	7.2	
			36MHz	8.8	3.9	

1. Typical values are measured at T_A=25 ℃ and V_{DD}= 3.3v.
2. Add an additional 0.8mA current consumption to each analog section of the ADC. In an application environment, this current is only increased when the ADC is turned on (setting the ON bit of the ADC_CTRL2 register).
3. External clock is 8MHz, PLL is enabled when f_{HCLK}>8MHz.

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Table 4-11 Typical current consumption in sleep mode

Symbol	Parameter	Condition	f_{HCLK}	Typ (1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Supply current in sleep mode	External clock(3)	144MHz	25.3	8	mA
			72MHz	13.9	5.3	
			36MHz	8	3.6	
		Run in high-speed internal RC oscillator (HSI), use AHB prescaler to reduce frequency.	128MHz	24.2	6.1	mA
			72MHz	13.9	3.5	
			36MHz	7.2	2.2	

1. Typical values are measured at T_A=25 ℃ and V_{DD}= 3.3v.
2. Add an additional 0.8mA current consumption to each analog section of the ADC. In an application environment, this current is only increased when the ADC is turned on (setting the ON bit of the ADC_CTRL2 register).
3. External clock is 8MHz, PLL is enabled when f_{HCLK}>8MHz.

4.3.6 External clock source characteristics

4.3.6.1 High-speed external clock source(HSE)

The characteristic parameters in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage refer to the conditions specified in Table 4-3.

Table 4-12 High speed external user clock characteristics(Bypass mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency(1)	-	4	8	32	MHz
V_{HSEH}	OSC_IN input pin high voltage		$0.8V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$	The time when OSC_IN is high or low(1)		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	The rising or falling time of OSC_IN(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitive reactance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	duty cycle	-	45	-	55	%
I_L	OSC_IN input leakage current	$V_{SS}≤V_{IN}≤V_{DD}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

4.3.6.2 Low-speed external clock source(LSE)

The characteristic parameters given in the following table are measured using a low speed external clock source, and the ambient temperature and supply voltage refer to the conditions specified in Table 4-3.

Table 4-13 Low-speed external user clock characteristics(Bypass mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency(1)	-	1	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low voltage		V_{SS}	-	200	mV
$t_{w(LSE)}$	The time when OSC32_IN is high or low(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	The rising or falling time of OSC32_IN(1)		-	-	50	
$DuCy_{(LSE)}$	duty cycle	-	30	-	70	%
I_L	OSC32_IN input leakage current	$V_{SS}≤V_{IN}≤V_{DD}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

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Figure 4-5 AC timing diagram of external high-speed clock source

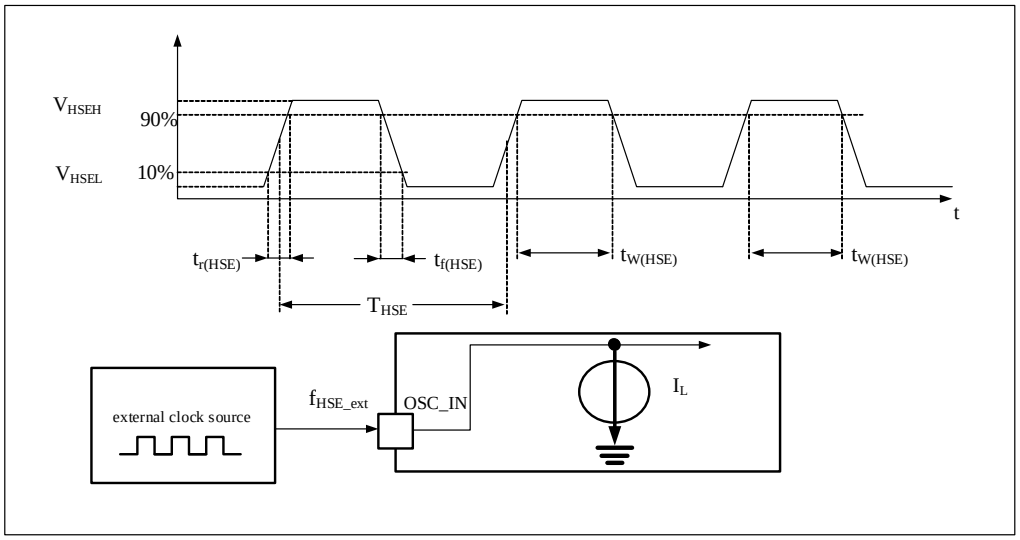
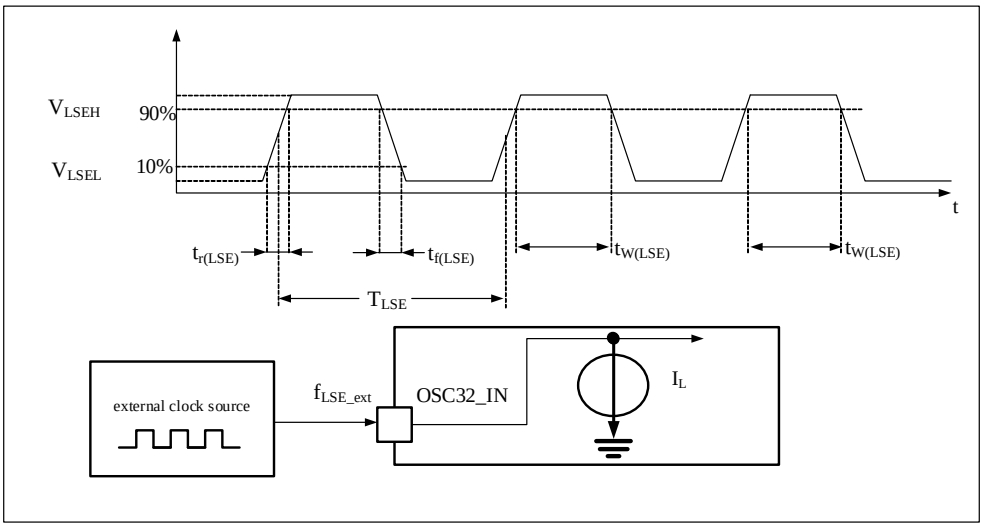


Figure 4-6 AC timing diagram of external low-speed clock source



High-speed external clock generated using a crystal/ceramic resonator

High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator).

Table 4-14 HSE 4~32MHz oscillator characteristics(1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	160	-	kΩ
i_2	HSE driving current	V_{DD}=3.3V,V_{IN}=V_{SS} 30pF load	-	1.3	1.6	mA
g_m	Oscillator transconductance	Startup	-	10	-	mA/V
$t_{SU(HSE)}$ (3)	Start time(8M crystal)	V_{DD} is stabilized	-	3	5	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, it is not tested in production.
3. $t_{SU(HSE)}$ is the start time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

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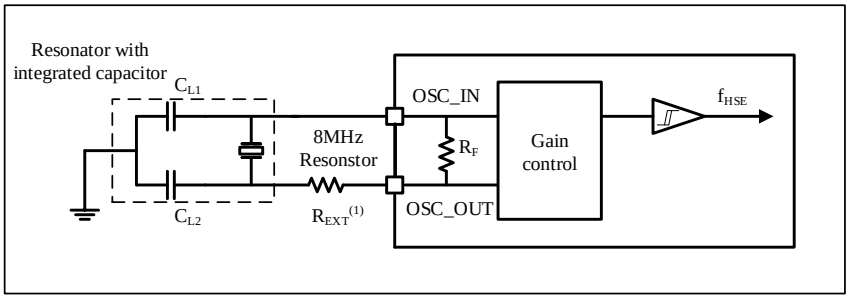
Figure 4-7 Typical application using 8MHz crystal



1. The REXT value depends on the properties of the crystal.

Low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768KHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Note: For C_{L1} and C_{L2}, it is recommended to use high quality ceramic dielectric containers. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2}.

Load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} /(C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

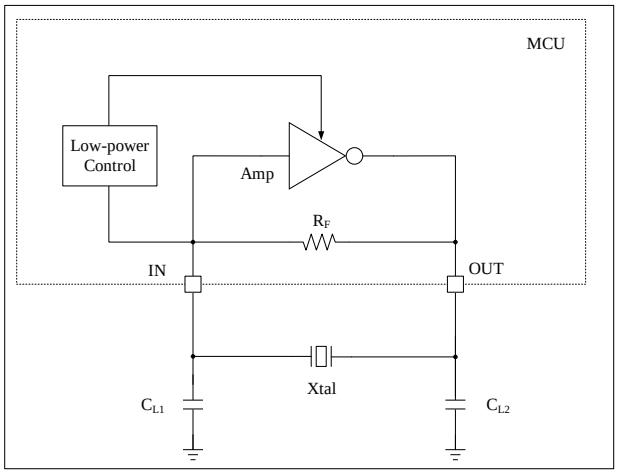
For example, if a resonator with a load capacitance of C_L=6pF is selected and C_{stray}=2pF, then C_{L1}=C_{L2}=8pF.

Table 4-15 LSE oscillator characteristics (f_{LSE}=32.768kHz)(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_F	Feedback resistance	-	-	5	-	MΩ
g_m	Oscillator transconductance	-	5	-	-	μA/V
$t_{SU(LSE)}$(2)	Startup time	V_{DD} is stabilized	-	2	-	s

1. According to the comprehensive evaluation, it is not tested in production.
2. $T_{SU(LSE)}$ is the startup time, which is the period from the LSE enabled by the software to the stable 32.768kHz oscillation. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-8 Typical application using 32.768kHz crystal(1) (2)



1. Please refer to the Crystal Selection Guide.
2. To ensure the working stability of the crystal, do not flip the adjacent pins when the crystal is working.

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4.3.7 Internal clock source characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with Table 4-3.

4.3.7.1 High speed internal (HSI) RC oscillator

Table 4-16 HSI oscillator characteristics(1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	V_{DD} =3.3V, T_A = 25℃, after calibration	7.92(3)	8	8.08(3)	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Temperature drift of HSI oscillator(4)	V_{DD} =3.3V， T_A= 0~70 ℃, temperature drift	-1.3	-	2	%
		V_{DD} =3.3V， T_A = -10~85℃, temperature drift	-2	-	2.2	%
		V_{DD} =3.3V， T_A= -40~105 ℃, temperature drift	-3	-	3	%
$t_{SU(HSI)}$	HSI oscillator start-up time	-	1	-	3	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	40	100	μA

1. V_{DD}= 3.3V, T_A=-40 ~ 105 ℃, unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Production calibration accuracy, excluding welding effects. Welding brings about +1.5% frequency deviation range.
4. Frequency deviation includes the effect of welding, data is from sample testing, not tested in production.

4.3.7.2 Low speed internal (LSI) RC oscillator

Table 4-17 LSI oscillator characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	Output frequency	25 ℃ calibration, VDD =3.3V	38	40	42	KHz
		VDD =1.8V ~3.6V, T_A = -40~105 ℃	30	48	60	KHz
$t_{SU(LSI)}$ (2)	LSI oscillator start-up time	-	-	30	80	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	0.2	-	μA

1. V_{DD}= 3.3V, T_A=-40 ~ 105 ℃, unless otherwise specified.
2. Guaranteed by design, not tested in production.

4.3.8 Wake up time from low power mode

The wake-up time listed in Table 4-18 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP0/STOP2/STANDBY mode: Clock source is RC oscillator.
- SLEEP mode: Clock source is the clock used when entering SLEEP mode.

All times were measured using ambient temperature and supply voltage in accordance with Table 4-3.

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Table 4-18 Wake-up time in low power mode

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$ (1)	Wake up from SLEEP mode	480	ns
$t_{WUSTOP0}$ (1)	Wake up from STOP0 (voltage regulator is in running mode)	20	µs
	Wake up from STOP 0 (voltage regulator is in low power mode)	22	
$t_{WUSTOP2}$ (1)	Wake up from STOP2	40	
$t_{WUSTDBY}$ (1)	Wake up from STANDBY mode	100	

1. The wake-up time is measured from the start of the wake-up event to the first instruction read by the user program.

4.3.9 PLL characteristic

The parameters listed in Table 4-19 are measured when the ambient temperature and power supply voltage refer to the conditions in Table 4-3.

Table 4-19 PLL characteristic

Symbol	Parameter	Value			Unit
		Min	Typ	Max (1)	
f_{PLL_IN}	PLL input clock(2)	4	8.0	32	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock	32	-	144	MHz
t_{LOCK}	PLL Ready indicates the signal output time.	-	-	150	µs
Jitter	Rms cycle-to-cycle jitter @144MHz	-	5	-	ps
Ipll	Operating Current of PLL @144MHz VCO frequency.	-	-	850	µA

1. Based on comprehensive evaluation, not tested in production.
2. Care needs to be taken to use the correct frequency doubling factor to input the clock frequency according to PLL so that f_{PLL_OUT} is within the allowable range.

4.3.10 FLASH memory characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A= -40~105 ℃.

Table 4-20 Flash memory characteristics

Symbol	Parameter	Condition	Min(1)	Typ (1)	Max(1)	Unit
tprog	32-bit programming time	T_A = -40~105 ℃	-	112	225	µs
t_{ERASE}	Page (2K bytes) erase time	T_A = -40~105 ℃	-	2	20(2)	ms
					100(3)	
t_{ME}	Whole erase time	T_A = -40~105 ℃;	-	-	100	ms
I_{DD}	Power supply current	Read mode, f_{HCLK}=144MHz,4 waiting cycles, V_{DD}=3.3V	-	-	3.62	mA
		Write mode, f_{HCLK}=144MHz, V_{DD}=3.3V	-	-	6.5	mA
		Erase mode, f_{HCLK}=144MHz, V_{DD}=3.3V	-	-	4.5	mA
		Power-down mode/shutdown, V_{DD}= 3.3 ~ 3.6V.	-	-	0.035	µA
Vprog	Programming voltage	-	1.8	3.0	3.6	V

1. Guaranteed by design, not tested in production.
2. Memory space with 10k erase times
3. Memory space with 100k erasing times

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Table 4-21 Flash endurance and data retention

Symbol	Parameter	Condition	Min(1)	Unit
N_{END}	Endurance (Note: number of erasures)	T_A =-40 ~ 105 ℃ ; The Flash capacity is 256KB.	10	Thousand times
		T_A =-40 ~ 105 ℃; The Flash capacity is 512KB, of which the first 256KB of storage space	10	
		T_A =-40 ~ 105 ℃; The Flash capacity is 512KB, including the last 256KB of storage space.	100	
t_{RET}	Data retention period	T_A= 85 ℃	20	year

1. Based on comprehensive evaluation, not tested in production.

4.3.11 Absolute maximum (electrical sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-22 Absolute maximum ESD value

Symbol	Parameter	Condition	Type	Min(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = +25 ℃, In accordance with MIL-STD-883K Method 3015.9	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = +25 ℃, In accordance with ESDA/JEDEC JS-002-2018	C3	1000	

1. Based on comprehensive evaluation, not tested in production.

Static latch-up

In order to evaluate the latch-up performance, two complementary static latching tests need to be performed on 6 samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78A integrated circuit latch-up standard.

Table 4-23 Electrical sensitivity

Symbol	Parameter	Condition	Type	Min(1)
LU	Static latch-up type	T_A = +25 ℃ , in accordance with JESD78A	Class II A	±100mA, 1.5*V_{DDMAX}

1. Test at room temperature.

4.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in Table 4-3. All I/O ports are CMOS and TTL compatible.

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Table 4-24 I/O static characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL port	Vss	-	0.8	V
V_{IH}	Input high level voltage		2	-	V_{DD}	
V_{IL}	Input low level voltage	CMOS port	Vss	-	0.35 V_{DD}	
V_{IH}	Input high level voltage		0.65 V_{DD}	-	V_{DD}	
Vhys	Schmitt trigger voltage hysteresis(1)	V_{DD}=3.3V	200	-	-	mV
		V_{DD}=2.5V	200	-	-	
		V_{DD}=1.8V	0.1*V_{DD}(2)	-	-	
I_{lkg}	Input leakage current(3)	V_{DD}=Maximum V_{PAD}=0 or V_{PAD}=V_{DD}(5)	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistance(4)	V_{DD}=3.3V,V_{IN}= V_{SS}	75	-	220	kΩ
		V_{DD} =2.5V, V_{IN} = V_{SS}	95	-	310	
		V_{DD} = 1.8V, V_{IN} = V_{SS}	135	-	500	
R_{PD}	Weak pull-down equivalent resistance(4)	V_{DD}=3.3V,V_{IN}= V_{DD}	75	-	235	kΩ
		V_{DD} = 2.5V, V_{IN} = V_{DD}	85	-	315	
		V_{DD} = 1.8V, V_{IN} = V_{DD}	120	-	495	
C_{IO}	Capacitance of I/O pin	-	-	5	-	pF

1. Hysteresis voltage of Schmitt trigger switch level. Based on comprehensive evaluation, not tested in production.
2. At least 100mV.
3. If there is reverse current backflow at the adjacent pins, the leakage current may be higher than the maximum value.
4. Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.
5. V_{PAD} refers to the input voltage of the IO pin.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

- For VIH:

  If VDD is between [1.8V ~ 3.08V]; Uses CMOS features but includes TTL.

  If VDD is between [3.08V ~ 3.60V]; Uses TTL feature but includes CMOS.

- For VIL:

  If VDD is between [1.8V ~ 2.28V]; Uses TTL feature but includes CMOS.

If VDD is between [2.28V ~ 3.60V]; Uses CMOS features but includes TTL.

Output drive current

GPIO (general purpose input/output port) can absorb or output up to +/-12mA current. In user applications, the number of I/O pins must ensure that the driving current does not exceed the absolute maximum rating given in Section 4.2:

- The sum of the current drawn from V_{DD} by all I/O ports, plus the maximum operating current drawn by the MCU on V_{DD}, cannot exceed the absolute maximum rating of I_{VDD} (Table 4-2).
- The sum of the current drawn by all I/O ports and drawn from V_{SS}, plus the maximum operating current drawn by the MCU on V_{SS}, cannot exceed the absolute maximum ratings, I_{VSS} (Table 4-2).

Output voltage

Unless otherwise specified, the parameters listed in Table 4-26were measured using ambient temperature and VDD supply voltage in accordance with Table 4-3. All I/O ports are CMOS and TTL compatible.

Table 4-25 IO driving capability Table

Driving grade	Condition	I_{OH}(1), VDD=3.3V	I_{OL}(1), VDD=3.3V	I_{OH}(1), VDD=2.5V	I_{OL}(1), VDD=2.5V	I_{OH}(1), VDD=1.8V	I_{OL}(1), VDD=1.8V	Unit
2	105℃	-2	2	-1.5	1.5	-1.2	1.2	mA
4	105℃	-4	4	-3	3	-2.5	2.5	
8	105℃	-8	8	-7	7	-5	5	
12	105℃	-12	12	-11	11	-7.5	7.5	

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1. Guaranteed by design, not tested in production.

Table 4-26 Output voltage characteristic

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}(1)	Output low level	V_{DD} = 3.3 V, drive level(4) 2/4/8/12	V_{SS}	0.55	V
		V_{DD} = 2.5 V, drive level(4) 2/4/8/12	V_{SS}	0.45	
		V_{DD} = 1.8 V, drive level(4) 2/4/8/12	V_{SS}	0.684	
V_{OH}(2)	Output high level	V_{DD} = 3.3 V, drive level(4) 2/4/8/12	2.4(3)	V_{DD}	
		V_{DD} = 2.5 V, drive level(4) 2/4/8/12	1.8(3)	V_{DD}	
		V_{DD} = 1.8 V, drive level(4) 2/4/8/12	0.8*V_{DD}	V_{DD}	

1. The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS}.
2. The current I_{IO} output from the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.
3. PC13, PC14 and PC15 are not in this range.
4. See Table 4-25 for actual driving capacity.

Input-output AC characteristics

The definitions and values of input and output AC characteristics are shown in Figure 4-9 and Table 4-27.

Unless otherwise specified, the parameters listed in Table 4-27 were measured using ambient temperature and supply voltage in accordance with Table 4-3.

Table 4-27 Output AC Characteristics(1)

DS_CFGy Configuration	PMODEy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
0	xx (2mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=5pF,V_{DD}=3.3V	-	75	MHz
				C_L=5pF,V_{DD}=2.5V	-	50	
				C_L=5pF,V_{DD}=1.8V	-	30	
		$t_{(IO)out}$	Output delay	C_L=5pF,V_{DD}=3.3V	-	3.66	ns
				C_L=5pF,V_{DD}=2.5V	-	4.72	
				C_L=5pF,V_{DD}=1.8V	-	7.12	
		$t_{(IO)in}$	Input delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	ns
1	00/01 (4mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 10pF, V_{DD}= 3.3V	-	90	MHz
				C_L=10pF,V_{DD}=2.5V	-	60	
				C_L=10pF,V_{DD}=1.8V	-	40	
		$t_{(IO)out}$	Output delay	C_L= 10pF, V_{DD}= 3.3V	-	3.5	ns
				C_L=10pF,V_{DD}=2.5V	-	4.5	
				C_L=10pF,V_{DD}=1.8V	-	6.74	
		$t_{(IO)in}$	Input delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
1	10 (8mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 20pF, V_{DD}= 3.3V	-	100	MHz
				C_L=20pF,V_{DD}=2.5V	-	75	
				C_L=20pF,V_{DD}=1.8V	-	50	
		$t_{(IO)out}$	Output delay	C_L= 20pF, V_{DD}= 3.3V	-	3.42	ns
				C_L=20pF,V_{DD}=2.5V	-	4.73	
				C_L=20pF,V_{DD}=1.8V	-	6.53	
		$t_{(IO)in}$	Input delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
1	11 (12mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 30pF, V_{DD}= 3.3V	-	120	MHz
				C_L=30pF,V_{DD}=2.5V	-	90	
				C_L=30pF,V_{DD}=1.8V	-	60	
		$t_{(IO)out}$	Output delay	C_L= 30pF, V_{DD}= 3.3V	-	3.34	ns
				C_L=3pF,V_{DD}=2.5V	-	4.26	
				C_L=3pF,V_{DD}=1.8V	-	6.34	
		$t_{(IO)in}$	Input delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	

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1. I/O port speed can be configured by DS_CFGy and PMODEy[1:0]. See N32A455 Series User Manual for the description of GPIO port configuration register.
2. The maximum frequency is Figure 4-9 Define.

Figure 4-9 Input output AC characteristic definition

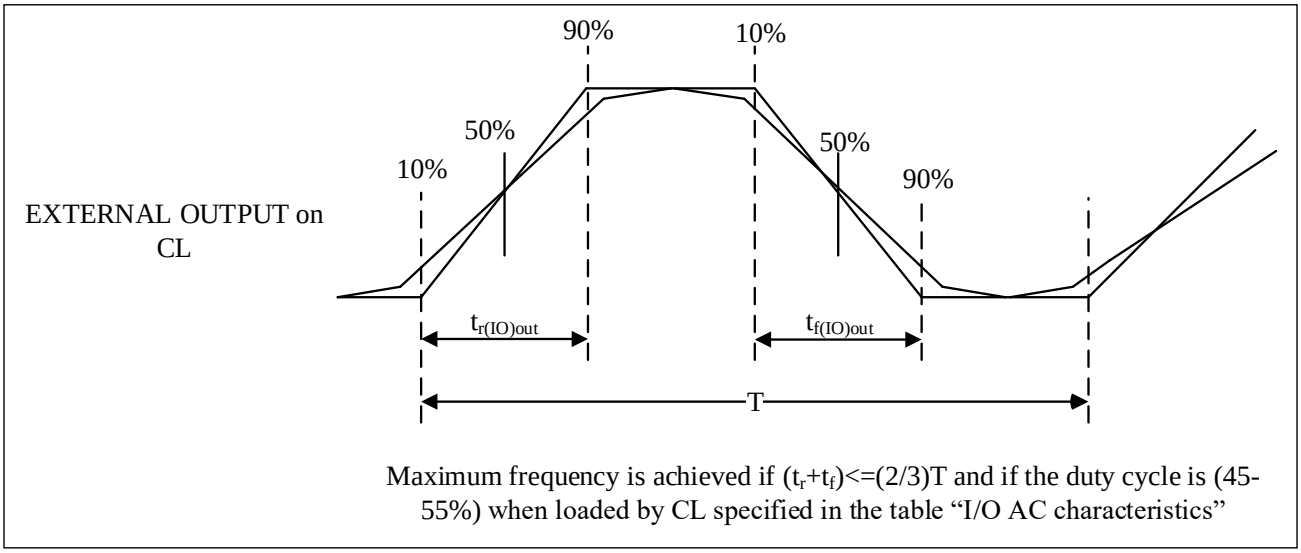
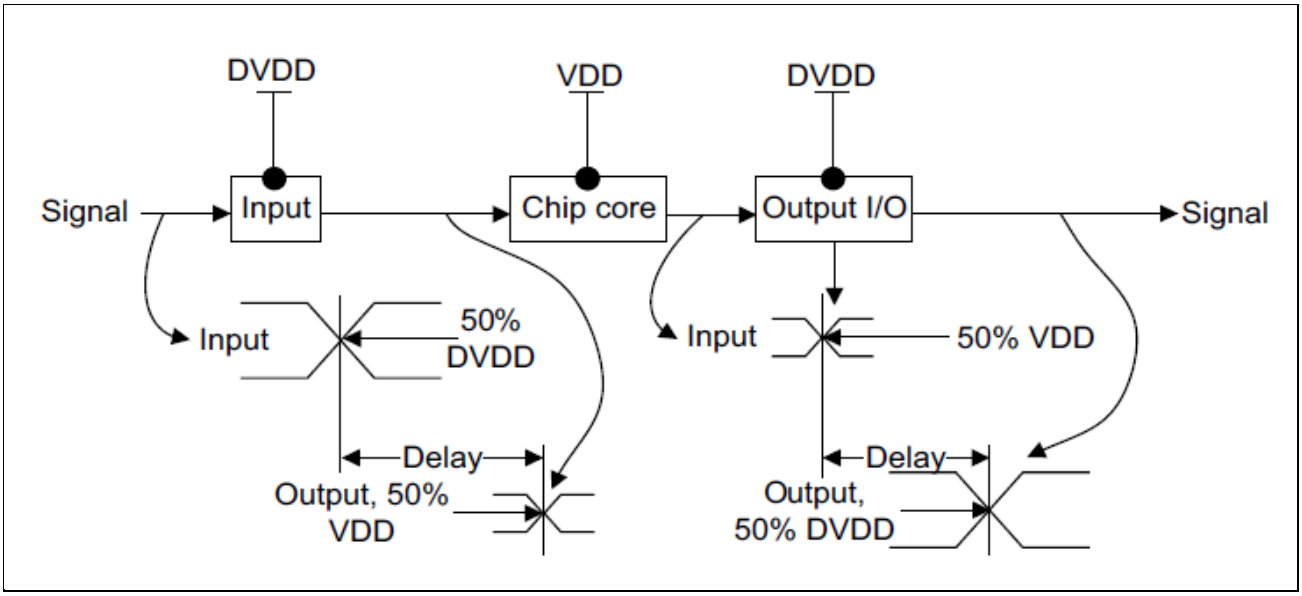


Figure 4-10 Transmission delay



4.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology and integrates a pull-up resistor that cannot be disconnected, R_{PU} (see Table 4-28). Unless otherwise specified, the parameters listed in Table 4-28 are measured using the ambient temperature and supply voltage in accordance with the conditions in Table 4-3.

Table 4-28 NRST pin characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low voltage	V_{DD} = 3.3 V	Vss	-	0.8	V
		V_{DD} = 1.8 V	Vss	-	0.3* V_{DD}	
$V_{IH(NRST)}$(1)	NRST input high voltage	V_{DD} = 3.3 V	2	-	V_{DD}	
		V_{DD} = 1.8 V	0.7* V_{DD}	-	V_{DD}	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	200	-	-	mV
		V_{DD} = 1.8 V	0.1* V_{DD}	-	-	V

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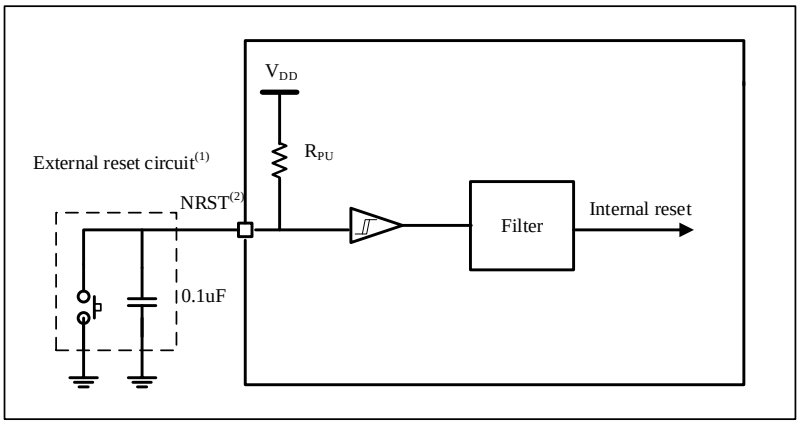
Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistance(2)	V_{DD} = 3.3 V	30	50	70	KΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is designed as a real resistor in series with a switchable PMOS. The resistance of this PMON/NMOS switch is very small (about 10%).

Figure 4-11 Recommended NRST pin protection for



1. Filter action.
2. The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in Table 4-28, otherwise the MCU cannot be reset.

4.3.14 Timer characteristics

I/O port characteristics for details on the features of the I/O reuse function pins (output comparison, input capture, external clock, PWM output), See section 4.3.12

Table 4-29 TIM1/8 characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	6.95	-	ns
f_{EXT}	Timer CH1 to CH4 external clock frequency	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 144MHz	0	72	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	0.00695	455	μs
t_{MAX_COUNT}	Maximum count	-	-	65536 x 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	-	29.8	s

1. Guaranteed by design, not tested in production.

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Table 4-30 TIM2/3/4/5 characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	13.9	-	ns
f_{EXT}	Timer CH1 to CH4 external clock frequency	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 72MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum count	-	-	65536 x 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	-	59.6	s

1. Guaranteed by design, not tested in production.

Table 4-31 IWDG counting maximum and minimum reset time (LSI = 40 KHz)

Prescaler	IWDG_PREDIV.PD[2:0]	Min(1) IWDG_RELV.REL[11:0]=0	Max(1) IWDG_RELV.REL[11:0]=0xFFF	Unit
/4	000	0.1	409.6	ms
/8	001	0.2	819.2	
/16	010	0.4	1638.4	
/32	011	0.8	3276.8	
/64	100	1.6	6553.6	
/128	101	3.2	13107.2	
/256	11x	6.4	26214.4	

1. Guaranteed by design, not tested in production.

Table 4-32 WWDG counting maximum and minimum reset time (APB1 PCLK1 = 36MHz)

Prescaler	WWDG_CFG.TIMERB[1:0]	Min(1) WWDG_CGF.W[6:0]=0x3F	Max(1) WWDG_CFG.W[6:0]=0x7F	Unit
/1	00	0.113	7.28	ms
/2	01	0.227	14.56	
/3	10	0.455	29.12	
/4	11	0.910	58.25	

1. Guaranteed by design, not tested in production.

4.3.15 I2C interface characteristics

Unless otherwise specified, the parameters listed in Table 4-33 were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with Table 4-3.

The I2C interface of the N32A455xxL7 product conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not "true" open leak pins, and when configured for open leak output, the PMOS tube between the pin and VDD is closed, but still exists.

I2C interface features are listed in Table 4-33. See Section 4.3.12 for details about the features of the input/output multiplexing function pins (SDA and SCL).

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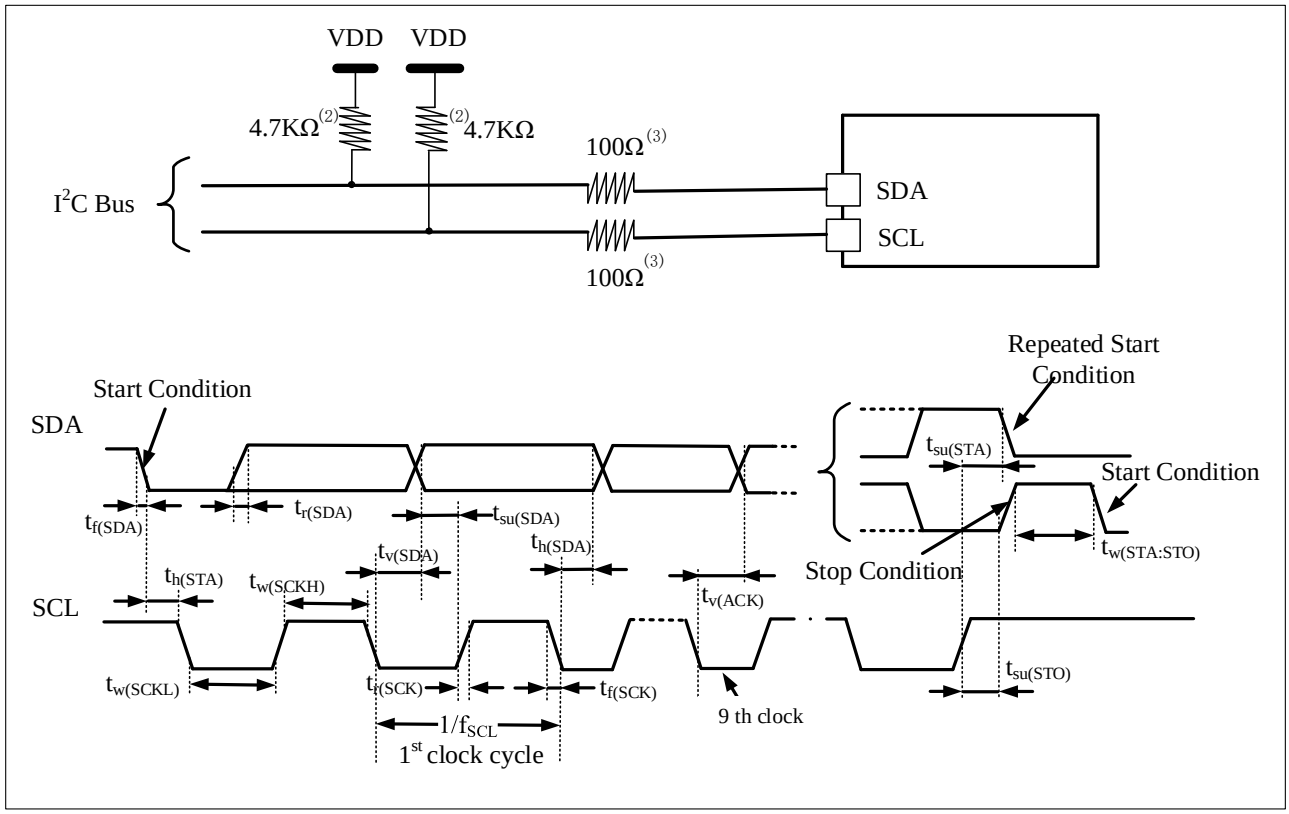
Table 4-33 I²C interface characteristics

Symbol	Parameter	Standard mode(1)(2)		Fast mode(1)(2)		Fast+ mode(1)(2)		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition holding time	4.0	-	0.6	-	0.26	-	μs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{su(STA)}$	Start condition establishment time of repetition	4.7	-	0.6	-	0.26	-	μs
$t_{h(SDA)}$	SDA data retention time	0	3.4	0	0.9	0	0.4	μs
$t_{su(SDA)}$	SDA setup time	250.0	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	20+0.1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL falling time	-	300	20+0.1Cb	300	-	120	ns
$t_{su(STO)}$	Stop condition establishment time	4.0	-	0.6	-	0.26	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.5	-	μs
Cb	Capacitive load per bus	-	400	-	400	-	100	pF
$t_{v(SDA)}$	Data validity time	-	3.45	-	0.9	-	0.45	μs
$t_{v\ (ACK)}$	Response effective time	-	3.45	-	0.9	-	0.45	μs

1. Guaranteed by design, not tested in production.
2. To achieve the maximum frequency of standard mode I²C, f_{PCLK1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I²C, f_{PCLK1} must be greater than 4MHz.
3. Above parameter conditions -40~105 ℃

Figure 4-12 I²C bus AC waveform and measurement circuit(1)



1. The measuring points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

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2. The pull-up resistor depends on the I2C interface speed.
3. The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.16 SPI/I²S interface characteristics

Unless otherwise specified, the SPI parameters listed in Table 4-34 / Table 4-35 and the I²S parameters listed in Table 4-36 are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with Table 4-3.

See section 4.3.12 for details on the characteristics of the I/O reuse pins (NSS, SCLK, MOSI, MISO for SPI, WS, CLK, SD for I²S).

Table 4-34 SPI1 feature(1)

Symbol	Parameter	Condition	Min	Max(105 ℃)	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	36	MHz
		Slave mode	-	36	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rise and fall time	Capacitance: C = 30pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI slave mode	45	55	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode	$t_{PCLK}-2$	$t_{PCLK}+2$	
$t_{su(MI)}$(1)	Enter the data setup time.	Master mode	3.5	-	
$t_{su(SI)}$(1)		Slave mode	3	-	
$t_{h(MI)}$(1)	Enter the data retention time	Master mode	3	-	
$t_{h(SI)}$(1)		Slave mode	3	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK}= 20MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$(1)(3)	Data output prohibition time	Slave mode	2	10	
$t_{v(SO)}$(1)	Data output effective time	Slave mode (after enabling edge)	-	12.5	
$t_{v(MO)}$(1)		Master mode (after enable edge)	-	6.5	
$t_{h(SO)}$(1)	Data output holding time	Slave mode (after enabling edge)	5	-	
$t_{h(MO)}$(1)		Master mode (after enable edge)	-0.5	-	

Table 4-35 SPI2/3 feature(1)

Symbol	Parameter	Condition		Min	Max(105 ℃)	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode		-	18	MHz
		Slave mode		-	18	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rise and fall time	Capacitance: C = 30pF		-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI slave mode		45	55	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode		$2t_{PCLK}$	-	
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode		$t_{PCLK}-2$	$t_{PCLK}+2$	
$t_{su(MI)}$(1)	Enter the data setup time.	Master mode	SPI2	4	-	
			SPI3	5	-	
$t_{su(SI)}$(1)		Slave mode	SPI2	4	-	

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			SPI3	5	-	
$t_{h(MI)}$(1)	Enter the data retention time	Master mode	SPI2	2	-	
			SPI3	2.5	-	
$t_{h(SI)}$(1)		Slave mode	SPI2	2	-	
			SPI3	2	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK}= 20MHz		0	$3t_{PCLK}$	
$t_{dis(SO)}$(1)(3)	Data output prohibition time	Slave mode		2	10	
$t_{v(SO)}$(1)	Data output effective time	Slave mode (after enabling edge)	SPI2	-	13.5	
			SPI3	-	17.5	
$t_{v(MO)}$(1)		Master mode (after enable edge)	SPI2	-	6.5	
			SPI3	-	9	
$t_{h(SO)}$(1)	Data output holding time	Slave mode (after enabling edge)	SPI2	4	-	
			SPI3			
$t_{h(MO)}$(1)		Master mode (after enable edge)	SPI2	1	-	
			SPI3			

1. Guaranteed by design, not tested in production.
2. The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.
3. The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

Figure 4-13 SPI timing diagram-slave mode and CLKPHA=0

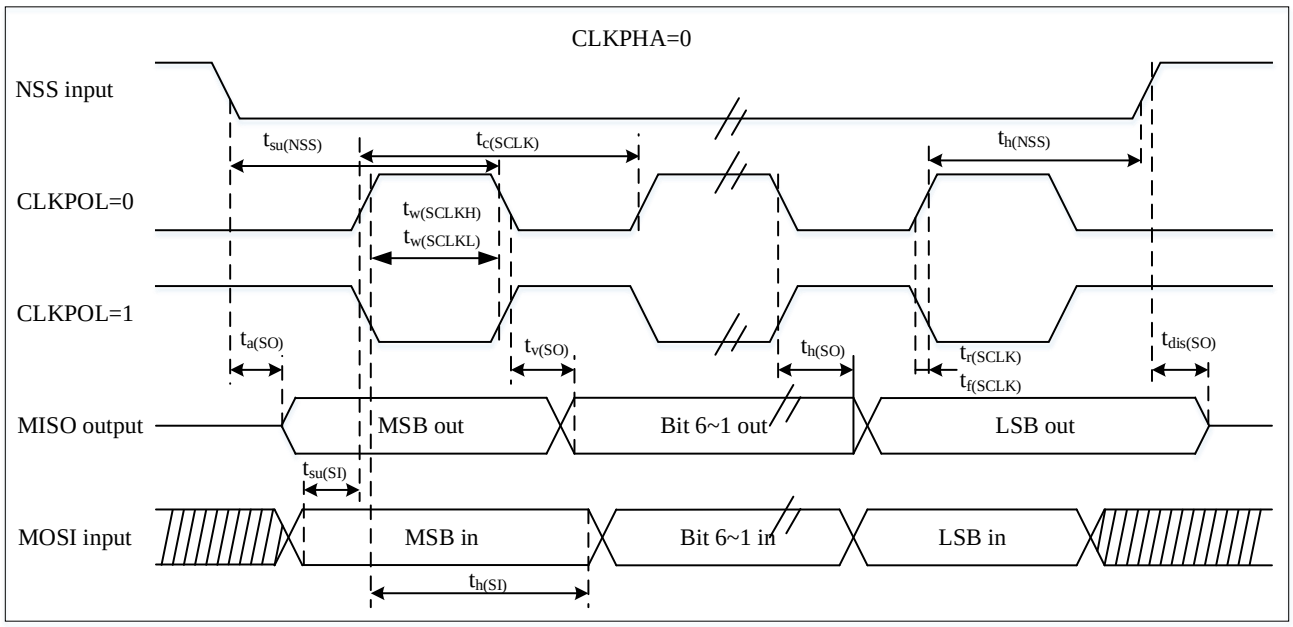

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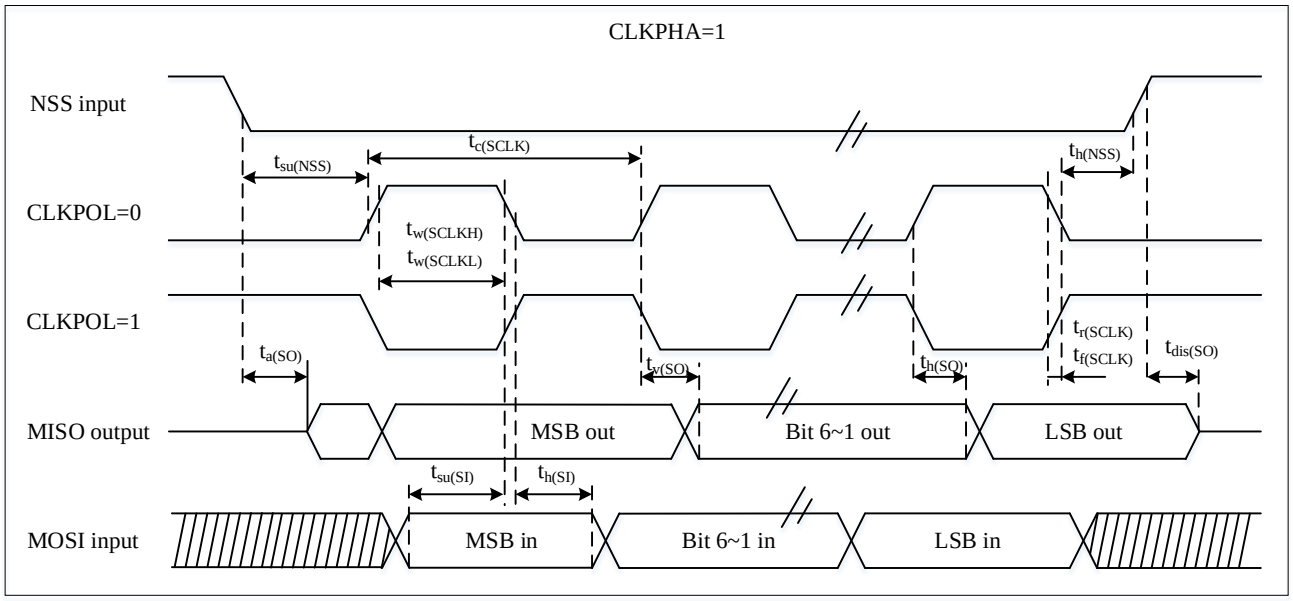
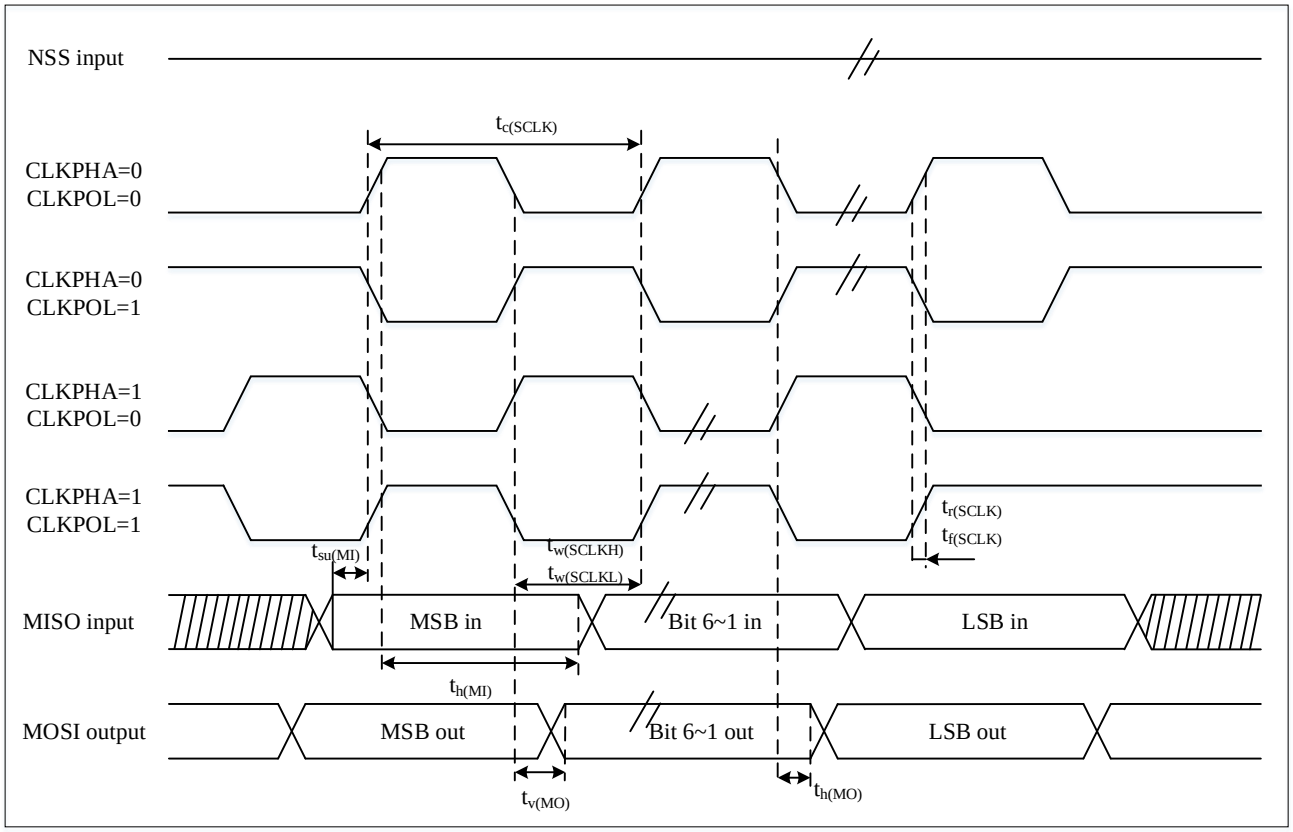
Figure 4-14 SPI timing diagram-slave mode and CLKPHA=1(1)



1. The measuring points is set at $0.3V_{DD}$and $0.7V_{DD}$.

Figure 4-15 SPI timing diagram-master mode(1)



1. The measuring points is set at $0.3V_{DD}$and $0.7V_{DD}$.

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Table 4-36 I²S characteristics(1)

Symbol	Parameter	Condition		Min	Max(105 ℃)	Unit
DuCy(SCK)	I²S slave input clock duty cycle	I2S slave mode		30	70	%
f_{MCLK}	I²S master clock	Master mode		-	256Fs(3)	MHz
f_{CLK} $1/t_{c(CLK)}$	I²S clock frequency	Master mode (32bit)		-	64*Fs(3)	
		Slave mode (32bit)		-	64*Fs(3)	
$t_{r(CLK)}$ $t_{f(CLK)}$	I²S clock rise and fall time	Capacitance: CL = 50pF		-	8	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	I2S2	4.5	-	
			I2S3	6.5	-	
$t_{h(WS)}$(1)	WS holding time	Master mode	I2S2	4.5	-	
			I2S3	0.5	-	
$t_{su(WS)}$(1)	WS setup time	Slave mode	I2S2	5.5	-	
			I2S3	7	-	
$t_{h(WS)}$(1)	WS holding time	Slave mode	I2S2	1.5	-	
			I2S3	2.5	-	
$t_{w(CLKH)}$(1)	CLK high and low time	Master mode, f_{PCLK}= 16MHz, audio frequency 48kHz		312.5	-	
$t_{w(CLKL)}$(1)				345	-	
$t_{su(SD\_MR)}$(1)	Enter the data setup time.	Master receiver	I2S2	4	-	
			I2S3	5	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	I2S2	4	-	
			I2S3	4.5	-	
$t_{h(SD\_MR)}$(1)(2)	Enter the data retention time	Master receiver	I2S2	1.5	-	
			I2S3	1.5	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	I2S2	1.5	-	
			I2S3	1.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output effective time	Slave transmitter (after enable edge)	I2S2	-	14	
			I2S3	-	16.5	
$t_{h(SD\_ST)}$(1)	Data output holding time	Slave generator (after enable edge)	I2S2	3.5	-	
			I2S3	4.5	-	
$t_{v(SD\_MT)}$(1)(2)	Data output effective time	Master generator (after enable edge)	I2S2	-	6.5	
			I2S3	-	6	
$t_{h(SD\_MT)}$(1)	Data output holding time	Master generator (after enable edge)	I2S2	-0.5	-	
			I2S3	-0.5	-	

1. Guaranteed by design, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK}=8MHz, then T_{PCLK}=1/f_{PCLK} =125ns.
3. Audio signal sampling frequency.

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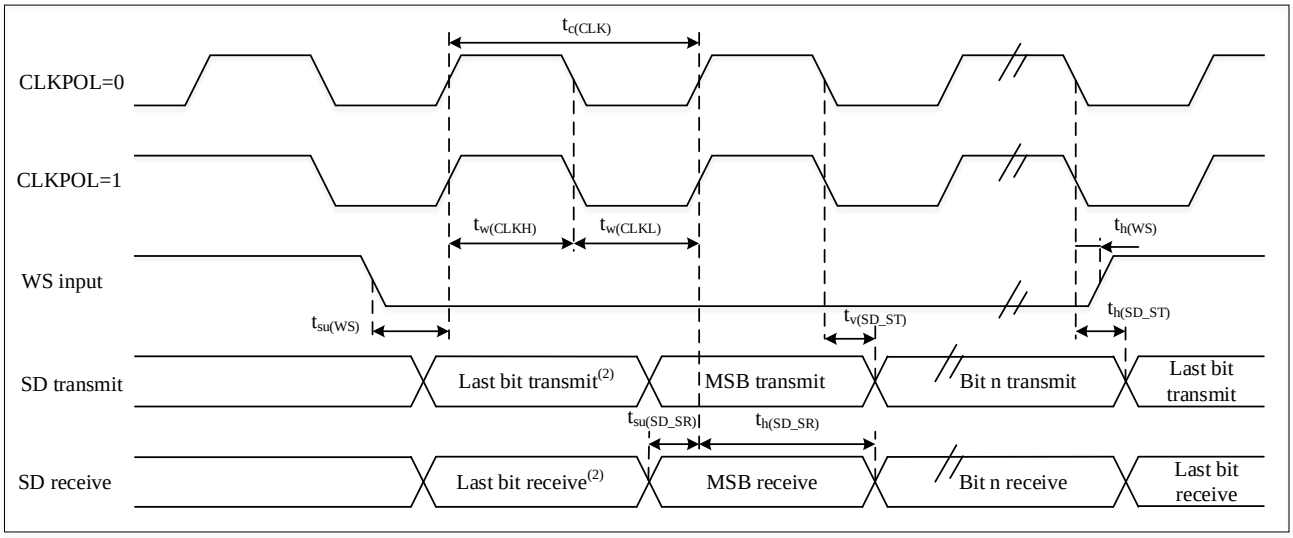
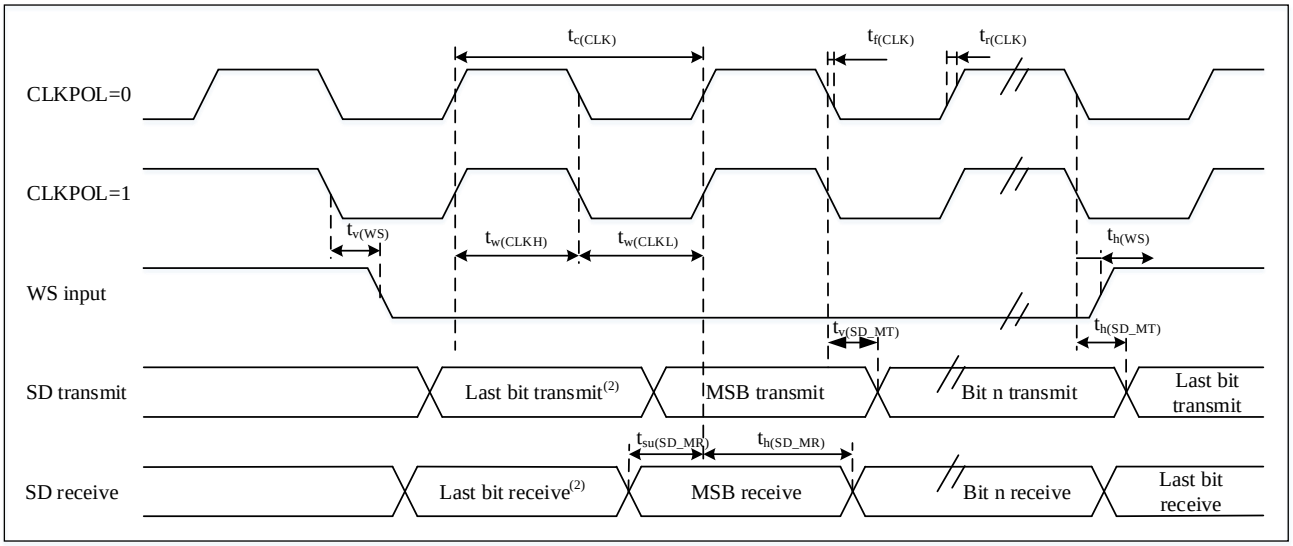
Figure 4-16 I²S slave mode timing diagram (Philips protocol)(1)



1. The measuring points is set at $0.3V_{DD}$and $0.7V_{DD}$.
2. Transmit/receive of the last byte. There is no transmit/receive of this least significant bit before the first byte.

Figure 4-17 I²S Master mode timing diagram (Philips Protocol)(1)



1. The measuring points is set at $0.3V_{DD}$and $0.7V_{DD}$.
2. Transmit/receive of the last byte. There is no transmit/receive of this last bit before the first byte.

4.3.17 QSPI characteristic

Table 4-37 Characteristics of QSPI in SDR mode

Symbol	Parameter	Min	Max(105 ℃)	Unit
f_{CK} $1/t_{(CK)}$	QSPI clock frequency	-	36	MHz
$t_{w(CKH)}$	SCK high and low time	$t_{(CK)}/2$-2	$t_{(CK)}/2$	ns
$t_{w(CKL)}$		$t_{(CK)}/2$	$t_{(CK)}/2$+2	ns
$t_{s(IN)}$	Enter data setup time.	4.5	-	ns
$t_{h(IN)}$	Enter the data retention time	4	-	ns
$t_{v(OUT)}$	Effective time of output data	-	5.5	ns
$t_{h(OUT)}$	Output data retention time	-0.15	-	ns

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Figure 4-18 Timing of QSPI in SDR mode

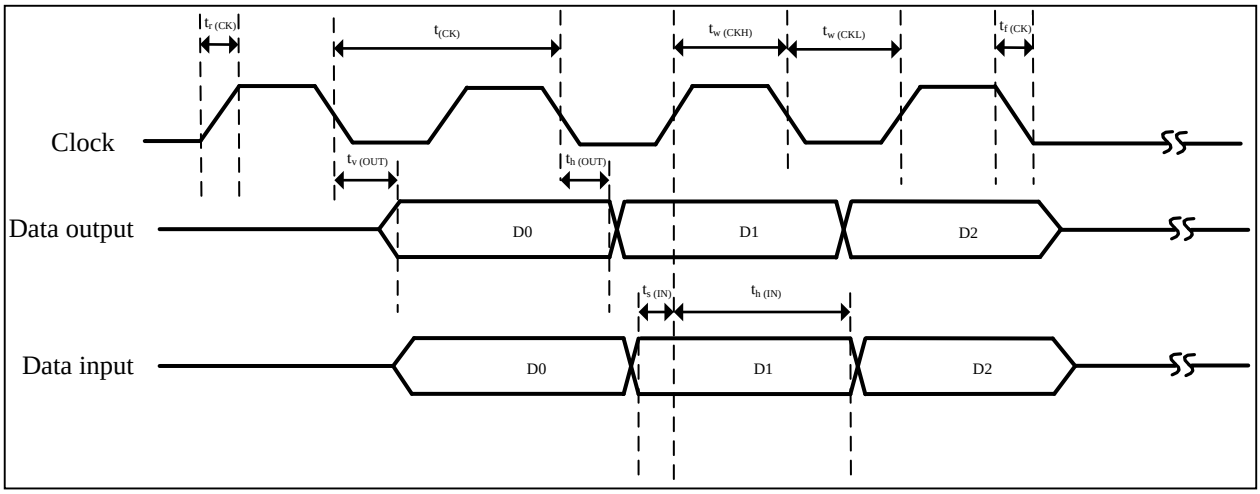
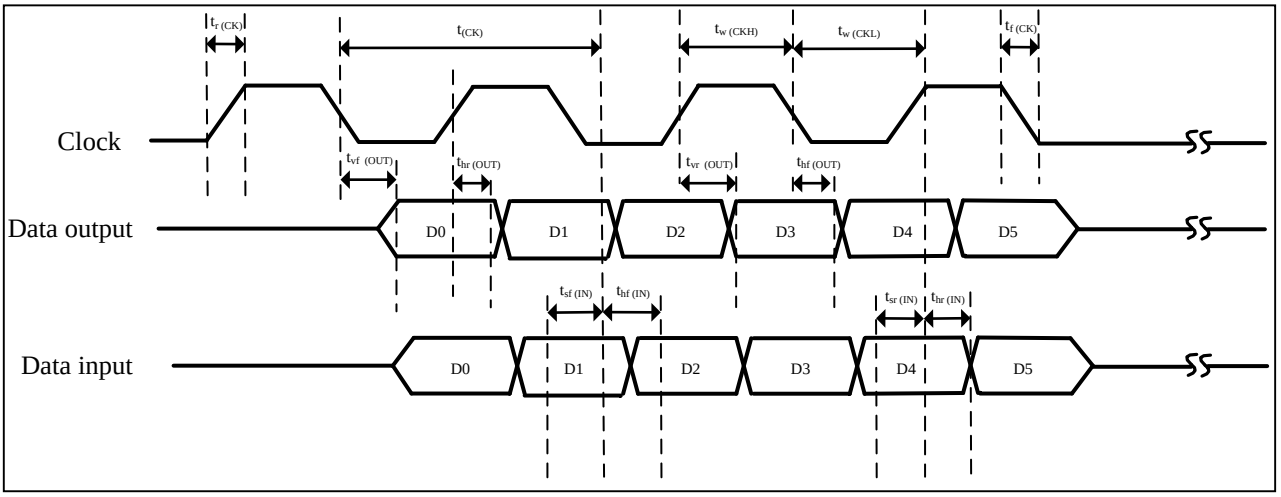


Table 4-38 Characteristics of QSPI in DDR mode

Symbol	Parameter	Min	Max(105 ℃)	Unit
f_{CK} $1/t_{(CK)}$	QSPI clock frequency	-	36	MHz
$t_{w(CKH)}$	SCK high and low time	$t_{(CK)}/2$-2	$t_{(CK)}/2$	ns
$t_{w(CKL)}$		$t_{(CK)}/2$	$t_{(CK)}/2$+2	ns
$t_{sf(IN)}$; $t_{sr(IN)}$	Enter data setup time.	4.5	-	ns
$t_{hf(IN)}$; $t_{hr(IN)}$	Enter the data retention time	4.5	-	ns
$t_{vf(OUT)}$; $t_{vr(OUT)}$	Effective time of output data	-	12	ns
$t_{hf(OUT)}$; $t_{hr(OUT)}$	Output data retention time	6	-	ns

Figure 4-19 Timing of QSPI in DDR mode



4.3.18 SD/SDIO host interface characteristics

Unless otherwise specified, the parameters listed in Table 4-39 are measured using ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage in accordance with the conditions in Table 4-3.

For details on the characteristics of the I/O alternate function pins (D[7:0], CMD, CK), see Section 4.3.12.

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Figure 4-20 SDIO high-speed mode

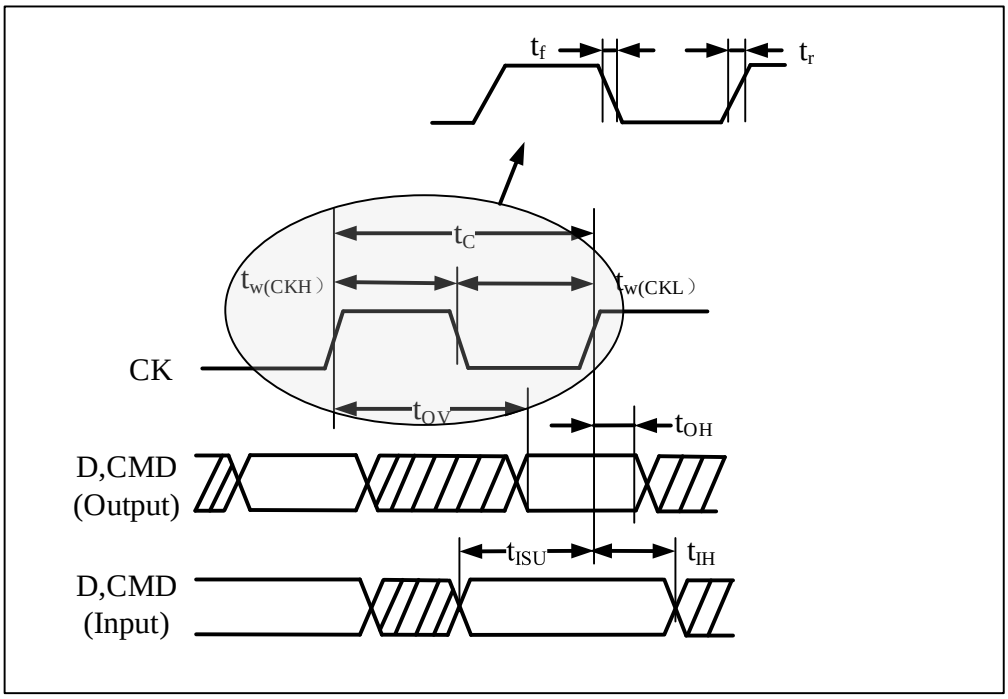

Figure 4-21 SD default mode

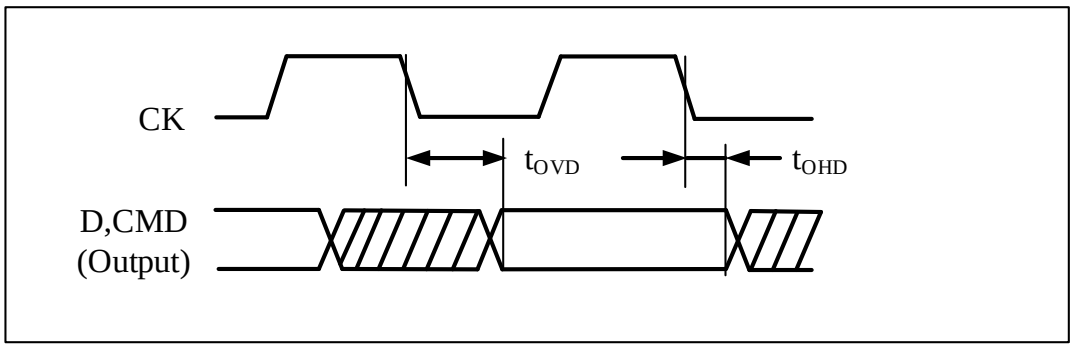

Table 4-39 SD/MMC interface features

Symbol	Parameter	Condition	Min	Max(105 ℃)	Unit
f_{PP}	Clock frequency in data transmission mode	CL ≤ 30pF	0	48	MHz
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	CL ≤ 30pF	32	-	ns
$t_{W(CKH)}$	Clock high time	CL ≤ 30pF	30	-	
t_r	Clock rising time	CL ≤ 30pF	-	6	
t_f	Clock falling time	CL ≤ 30pF	-	6	
CMD, D input (refer to CK)					
t_{ISU}	Enter the setup time.	CL ≤ 30pF	1	-	ns
t_{IH}	Enter holding time	CL ≤ 30pF	1	-	
CMD, D output in MMC and SD high-speed mode (refer to CK)					
t_{OV}	Output effective time	CL ≤ 30pF	-	6	ns
t_{OH}	Output holding time	CL ≤ 30pF	0	-	
CMD, D output in SD default mode (refer to CK)					
t_{OVD}	Output valid default time	CL ≤ 30pF	-	8	ns
t_{OHD}	Output hold default time.	CL ≤ 30pF	-1	-	

4.3.19 Characteristics of Controller Area Network (CAN) Interface

See Section 4.3.12 for details on the features of the input/output multiplexing function pins (CAN_TX and CAN_RX).

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4.3.20 Electrical parameters of 12-bit analog-to-digital converter (ADC)

Unless otherwise specified, the parameters in Table 4-40 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

Note : It is recommended to perform a calibration at each power up.

Table 4-40 ADC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	supply voltage	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	
f_{ADC}	ADC clock frequency	-	-	-	80	MHz
fs(2)	sampling rate	1.8V ≤ V_{DD} ≤ 3.6V, Resolution 12bit	0.01(2)	-	4.7(1)	MHz
		1.8V ≤ V_{DD} ≤ 3.6V, Resolution 10bit	0.012(2)	-	6.1(1)	MHz
		1.8V ≤ V_{DD} ≤ 3.6V, Resolution 8bit	0.014(2)	-	7.3(1)	MHz
		1.8V ≤ V_{DD} ≤ 3.6V, Resolution 6bit	0.0175(2)	-	8.9(1)	MHz
V_{AIN}	Convers ionvoltage range(3)	-	0(V_{IN} or V_{REF-} Connect to ground)	-	V_{REF+}	V
R_{ADC}(2)	Sampling switch resistance	Fast channel, Under the condition of 3.6V voltage	-	-	137.6	Ω
		Slow channel, Under the condition of 3.6V voltage	-	-	147	Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	5	-	pF
SNDR	Signal noise distortion ration	-	-	65	-	dBFS
T_{cal}	Calibration time	-	82			$1/f_{ADC}$
Ts(2)	Sampling cycles	Resolution 6/8/10/12-bit	1.5	-	601.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	6	10	20	μs
t_{CONV}(2)	Total conversion time of (including sampling time)	-	8~614 (sampling ts + gradually approaching 6.5/8.5/10.5/12.5)			$1/f_{ADC}$

1. Only fast channel support, f_{ADC} = 80 MHz.
2. Guaranteed by design, not tested in production.
3. According to different packages, V_{REF+} can be internally connected to V_{IN} and V_{REF-} can be internally connected to V_{IN}.

Formula 1: maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-41 ADC sampling time(1) (2)

Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time（ns）	Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time（ns）
Fast channel	12-bit	0.06	37	Slow channel	12-bit	0.05	53
		0.36	45			0.35	73
		0.86	79			0.85	103
		4.86	300			4.85	345

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Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time（ns）	Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time（ns）
		9.86	576			9.85	651
		19.86	1131			19.85	1257
		49.86	2776			49.85	3051
		99.86	5475			99.85	5982
Fast channel	10-bit	0.06	25	Slow channel	10-bit	0.05	46
		0.36	39			0.35	61
		0.86	64			0.85	88
		4.86	250			4.85	357
		9.86	478			9.85	540
		19.86	935			19.85	1040
		49.86	2294			49.85	2526
		99.86	4532			99.85	4963
Fast channel	8-bit	0.06	22	Slow channel	8-bit	0.05	39
		0.36	33			0.35	50
		0.86	52			0.85	71
		4.86	202			4.85	234
		9.86	391			9.85	457
		19.86	800			19.85	1012
		49.86	1838			49.85	2027
		99.86	3632			99.85	3984
Fast channel	6-bit	0.06	19	Slow channel	6-bit	0.05	32
		0.36	27			0.35	40
		0.86	41			0.85	56
		4.86	153			4.85	177
		9.86	292			9.85	330
		19.86	569			19.85	642
		49.86	1435			49.85	1666
		99.86	3001			99.85	3919

1. Guaranteed by design, not tested in production.
2. Typical values are measured at T_A=25 ℃ and V_{DD}= 3.3V.

Table 4-42 ADC accuracy-limited test conditions(1)(2)

Symbol	Parameter	Test condition	Typ	Max	Unit
ET	composite error	f_{HCLK} = 72 MHz,	±1.3	±5	LSB
EO	offset error	f_{ADC} = 72 MHz, sample rate=1.75Msps,	±1	±2	
ED	Differential linear error	V_{DDA} = 3.3V,T_A = 25 ℃	±0.7	±1	
EL	Integral linear error	The measurement is performed after ADC calibration. V_{REF+}= V_{DDA}	±0.8	±2	

1. The DC accuracy values of the ADC are measured after internal calibration.
2. ADC Accuracy vs. Reverse Injection Current: Injecting reverse current on any standard analog input pin needs to be avoided, as this will significantly degrade the accuracy of an ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to standard analog pins where reverse injection current may occur.
3. Guaranteed by comprehensive evaluation, not tested in production.

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Figure 4-22 ADC precision characteristics

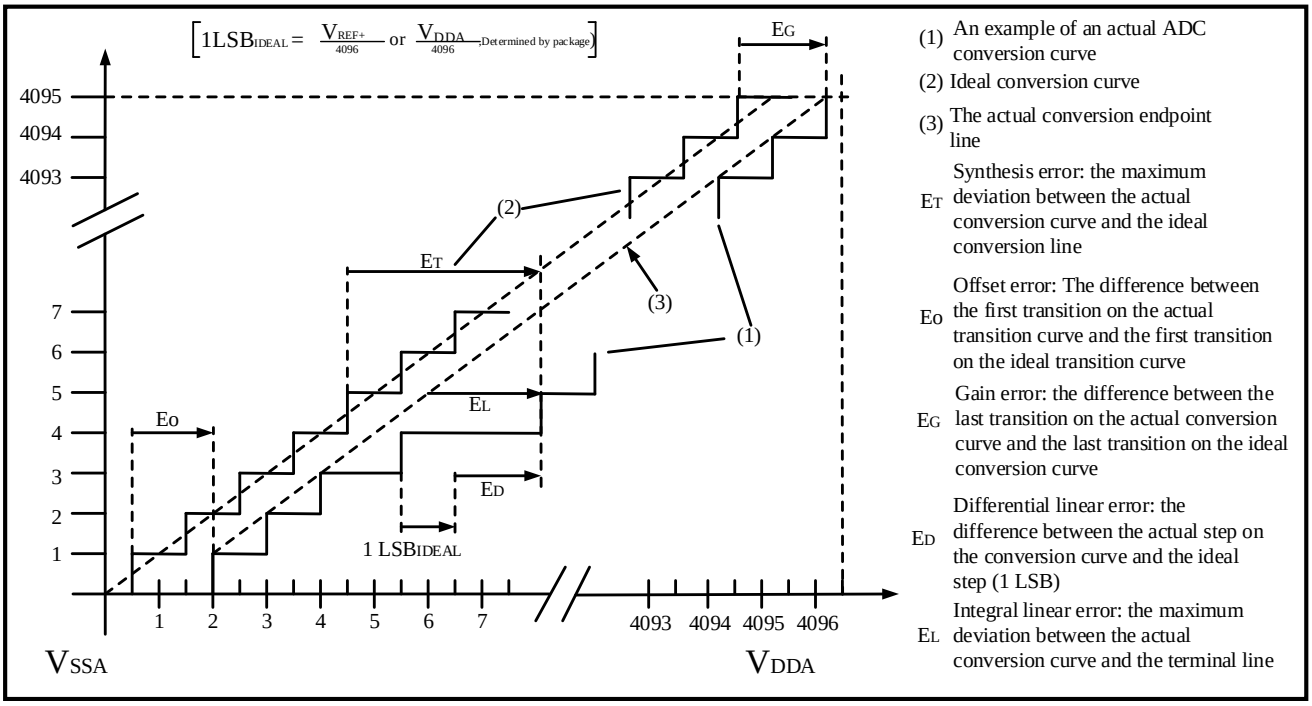
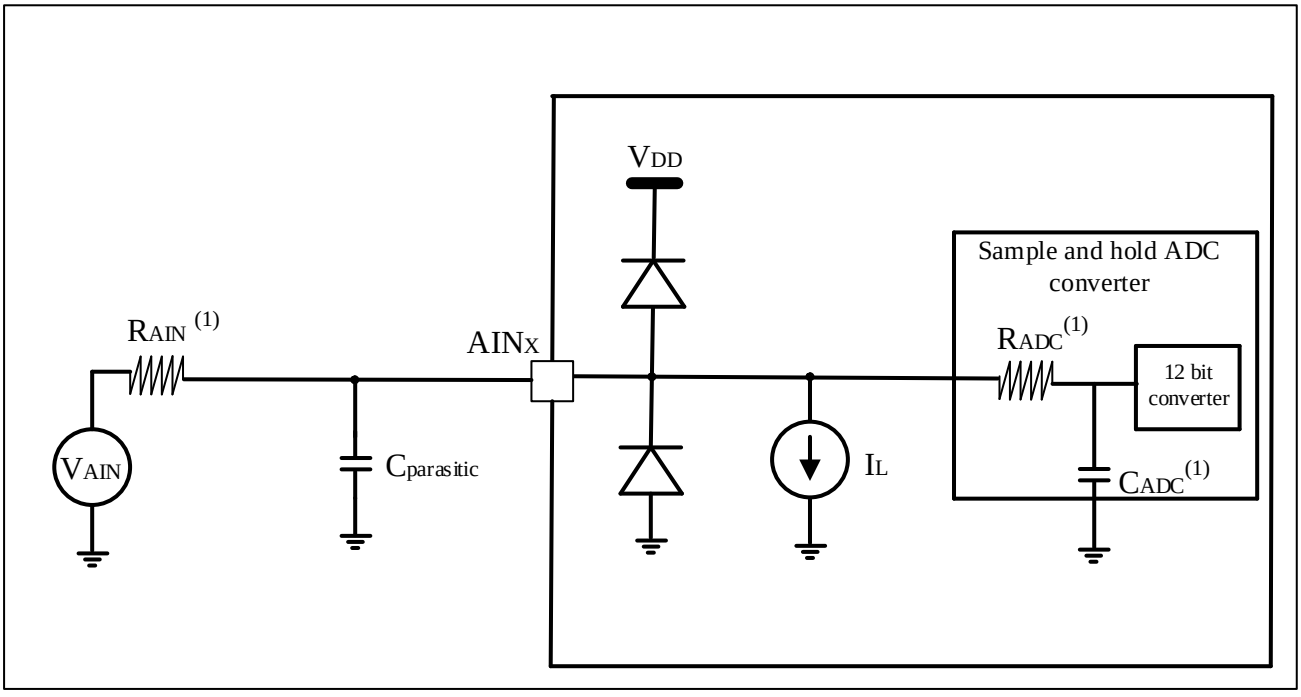


Figure 4-23 Typical connection diagram using ADC



1. On the numerical values of R_{AIN}, R_{ADC} and C_{ADC}, see Table 4-40.

Note: Cparasitic represents parasitic capacitance on PCB (related to soldering and PCB layout quality) and pads(approximately 7pF). A larger Cparasitic value would reduce the accuracy of conversion, and the solution was to reduce f_{ADC}.

PCB design suggestions

Depending on whether V_{REF+} is connected to V_{DDA}, the decoupling of the power supply must be connected as shown in Figure 4-24 or Figure 4-25. The 10nF capacitors in the picture must be ceramic capacitors (good quality), and they should be as close to the MCU chip as possible.

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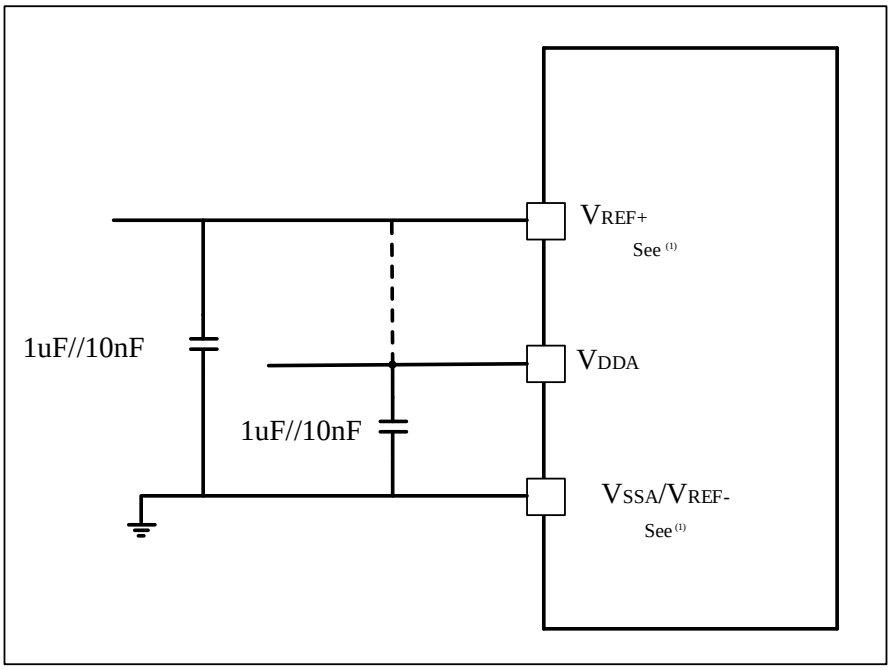
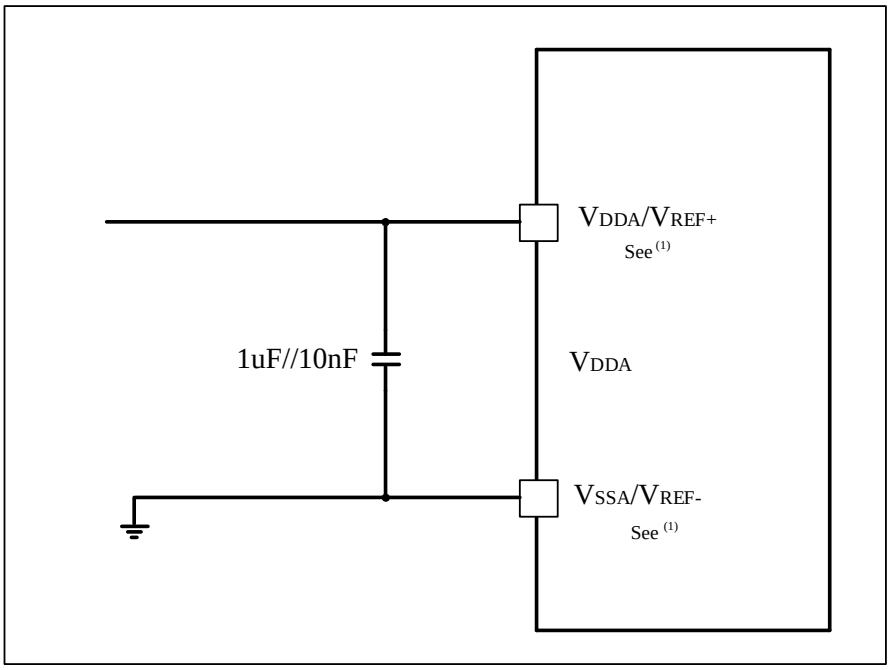
Figure 4-24 Decoupling circuit of power supply and reference power supply (V_{REF+} is not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs only products with more than 100 pins.

Figure 4-25 Decoupling circuit of power supply and reference power supply (V_{REF+} is connected with V_{DDA})



1. V_{REF+} and V_{REF-} inputs only products with more than 100 feet.

4.3.21 Electrical parameters of 12-bit digital-to-analog converter (DAC)

Unless otherwise specified, the parameters in Table 4-43 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

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Table 4-43 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Annotate
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{DDD}	Digital supply voltage	1.0	1.1	1.2	V	-
V_{REF+}	Reference voltage	2.4	-	3.6	V	V_{REF+} must always be lower than V_{DDA}
V_{SSA}	Ground wire	0	-	0	V	-
R_L	Load resistance when buffer is open	5	-	-	KΩ	The minimum load resistance between DAC_OUT and V_{SSA}
C_L	Load Capacitance	-	-	50	pF	Maximum capacitance on DAC_OUT pin
DAC_OUT minimum	DAC_OUT voltage when buffer is open	0.2	-	-	V	The maximum DAC output span is given. When V_{REF+}=3.6V corresponds to a 12-bit input value 0x0E0~0xF1C, When V_{REF+}=2.4V corresponds to a 12-bit input value 0x155~0xEAB.
DAC_OUT maximum	DAC_OUT voltage when buffer is open	-	-	V_{REF+} – 0.2	V	
	DAC_OUT voltage when buffer is closed	-	-	V_{REF+} – 5LSB		
I_{DD}	In static mode (standby mode), DAC DC consumption (V_{DDD}+V_{DDA}+V_{REF+})	-	425	600	μA	No load, enter the median 0x800
		-	500	700		No load, enter the maximum value when V_{REF+}= 3.6V.
I_{DDQ}	DC consumption of DAC in power-down mode (V_{DDD}+V_{DDA}+V_{REF+})	-	5	350	nA	non-loaded
	DC consumption of DAC in power-down mode (V_{DDA}+V_{REF+})	-	5	200		
DNL	Nonlinear distortion (deviation between two consecutive codes)	-	±0.5	-	LSB	DAC is configured with 10 bits (B1=B0=0 at all times)
		-	±2	-	LSB	DAC is configured with 12 bits
INL	Non-linearity accumulation (deviation between the measured value at code I and the line between code 0 and code 4095)	-	±6	-	LSB	DAC is configured as 12-bit
offset	Offset error (the deviation between the measured value of code 0x800 and the ideal value V_{REF+}/2)	-	±10	-	mV	DAC is configured as 12-bit
		-	±12	-	LSB	With V_{REF+}=3.6V, the DAC is configured with 12 bits.
Gain error	Gain error	-	±0.5	-	%	DAC is configured as 12-bit
Amplifier gain	Gain of open-loop amplifier	80	85	-	dB	The load of 5k (maximum load) , input medium value is 0x800
$t_{SETTLING}$	Setting time (full range: 10-bit input code changes from minimum value to maximum value, and DAC_OUT reaches ±1 LSB of its final value)	-	5	7	μs	C_{LOAD} ≤ 50pF R_{LOAD} ≥ 5kΩ
Update rate	When the input code changes slightly (from the value i to i+1LSB), the maximum frequency of the correct DAC_OUT is obtained.	-	-	1	MS/s	C_{LOAD} ≤ 50pF R_{LOAD} ≥ 5kΩ
t_{WAKEUP}	Time to wake up from off state (setting the CHxEN bit in DAC control register)	-	6.5	10	μs	C_{LOAD}≤ 50pF,R_{LOAD}≥ 5kΩ The input code is between the minimum and maximum possible values.
PSRR+	Power supply rejection ratio (relative to V_{DD}33A) (static DC measurement)	-	-67	-40	dB	Without R_{LOAD},C_{LOAD}≤ 50pF

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4.3.22 Electrical parameters of operational amplifier (OPAMP)

Unless otherwise specified, the parameters in Table 4-44 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

Table 4-44 OPAMP characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max(105 ℃)	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common-mode voltage input range	-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	-	-3.5	+/-1	3.5	mV
ΔVI_{OFFSET}	Input offset voltage temperature drift	-	-	10	-	μV/℃
I_{LOAD}	drive current	-	-	0.5	-	but
I_{DDA}	Operational amplifier current consumption	No load, quiescent mode	-	-	1.5	but
TS_OPAMP_VOUT	ADC sampling time as output of operational amplifier	-	400	-	-	ns
CMMR	common mode rejection ratio	-	-	84	-	dB
PSRR	Power supply rejection ratio	-	-	100	-	dB
GBW	Gain bandwidth	-	-	4	-	MHz
SR	conversion rate	-		1.5	-	V/μs
RLOAD	Minimum impedance load	-	4	-	-	KO
CLOAD	Maximum capacitive reactance load	-	-	-	50	pF
$T_{STARTUP}$	Setup time	CLOAD ≤ 50 pF, RLOAD ≥ 4 kΩ, Follower configuration	-	3	-	μs
PGA Gain error	Programmable gain error	Input signal amplitude> 10	-	±2.5	-	%
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	2	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 5 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 6 KΩ	-	0.25	-	
		PGA Gain = 32, Cload = 50pF, Rload = 7 KΩ	-	0.125	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	111	-	$nV/\sqrt{Hz}$
		@ 10KHz, Output loaded with 4 KΩ	-	43.9	-	

1. Guaranteed by design, not tested in production.

4.3.23 Electrical parameters of comparator (COMP)

Unless otherwise specified, the parameters in Table 4-45 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

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Table 4-45 COMP characteristic

Symbol	Parameter	Condition		Min	Typ	Max(105 ℃)	Unit
V_{DDA}	Analog supply voltage	-		1.8	-	3.6	V
V_{IN}	Input voltage range	-		0	-	V_{DDA}	
t_{START}(1)	Comparator startup setup time	-		-	10	-	μs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	-		-	70	-	ns
V_{OFFSET}	Comparator input offset error	Full common mode range		-	±10	-	mV
Vhys	Compare hysteresis voltage	No hysteresis		-	0	-	mV
		Low hysteresis		-	20	-	
		Medium hysteresis		-	30	-	
		High hysteresis		-	40	-	
I_{DDA}	Comparator current consumption	High speed mode	Static	-	50	-	μA
			With 50 kHz ±100 mV overdrive square signal	-	60	-	

1. Guaranteed by design, not tested in production.

4.3.24 Temperature sensor (TS) characteristics

Unless otherwise specified, the parameters in Table 4-46 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

Table 4-46 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max(105 ℃)	Unit
T_L(1)	Linearity of V_{SENSE} with respect to temperature	-	±1	±4	℃
Avg_Slope(1)	Average slope	-	-4.1	-	mV/ ℃
V_{30}(1)	Voltage at 30 ℃	-	1.32	-	V
t_{START}(1)	setting time	-	10	-	μs
T_{S_temp}(2)(3)	When reading temperature, ADC sampling time	8.3	-	-	μs

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time of can be determined by the application through multiple cycles.

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5 Package Information

5.1 LQFP48

Figure 5-1 LQFP48 package outline

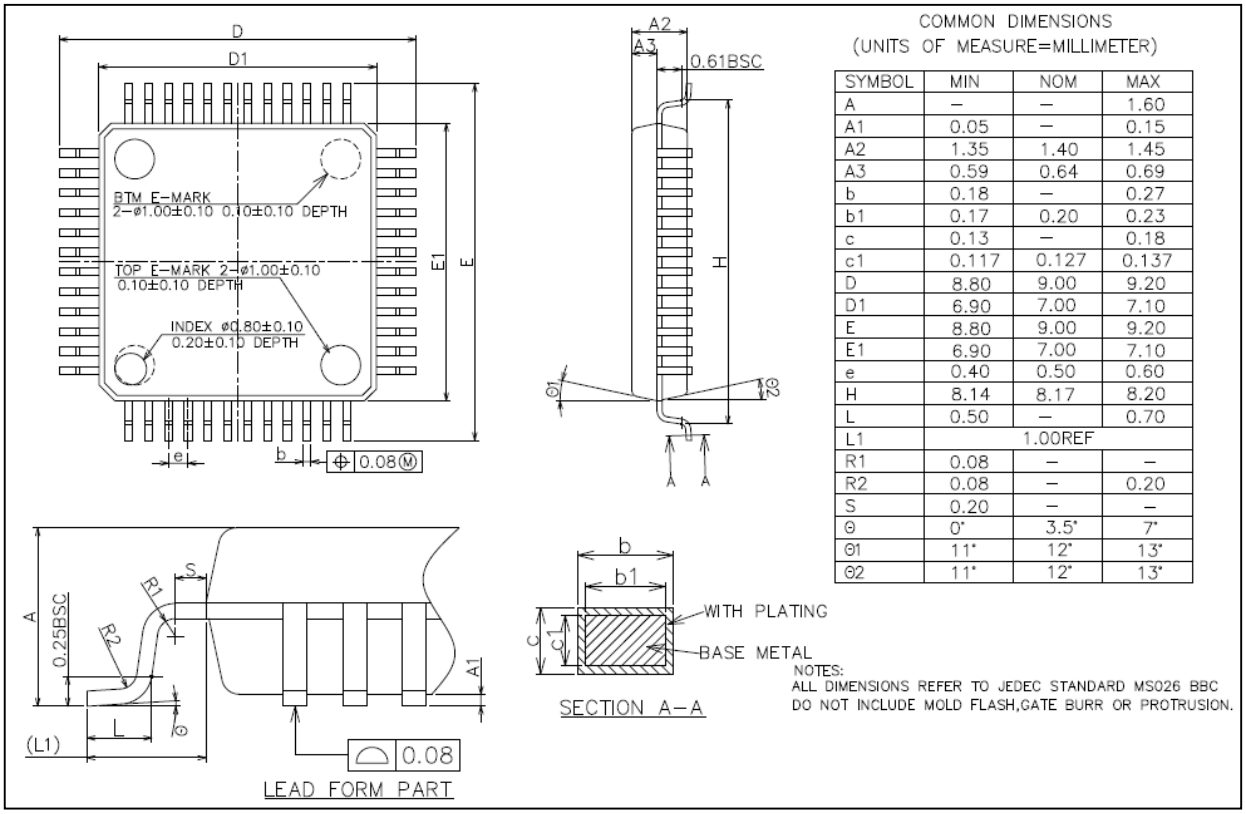
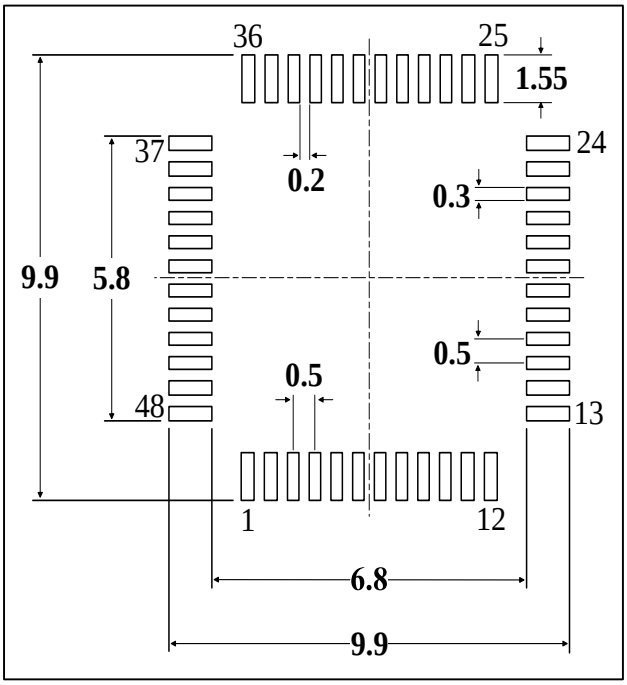


Figure 5-2 LQFP48 recommended footprint (1)



1. Dimensions are expressed in millimeters.

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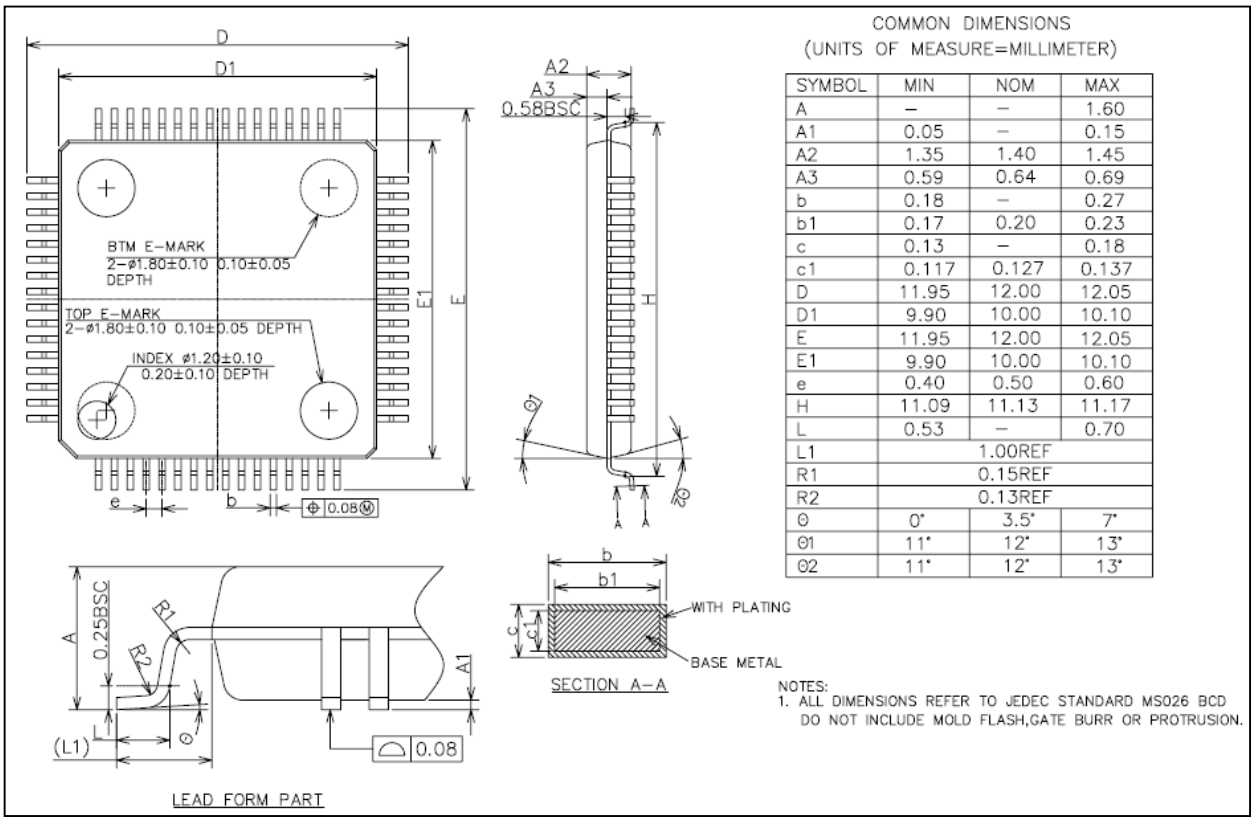
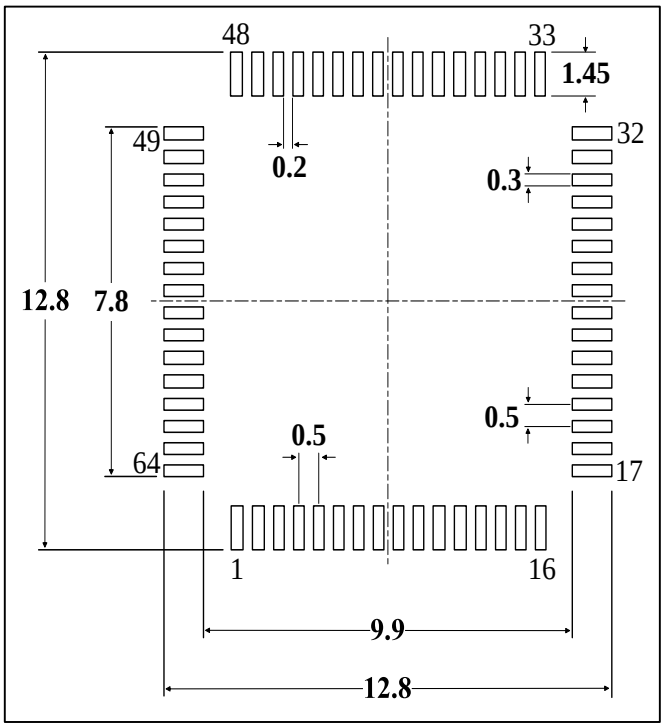
5.2 LQFP64

Figure 5-3 LQFP64 package outline



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

Figure 5-4 LQFP64 recommended footprint (1)



1. Dimensions are expressed in millimeters.

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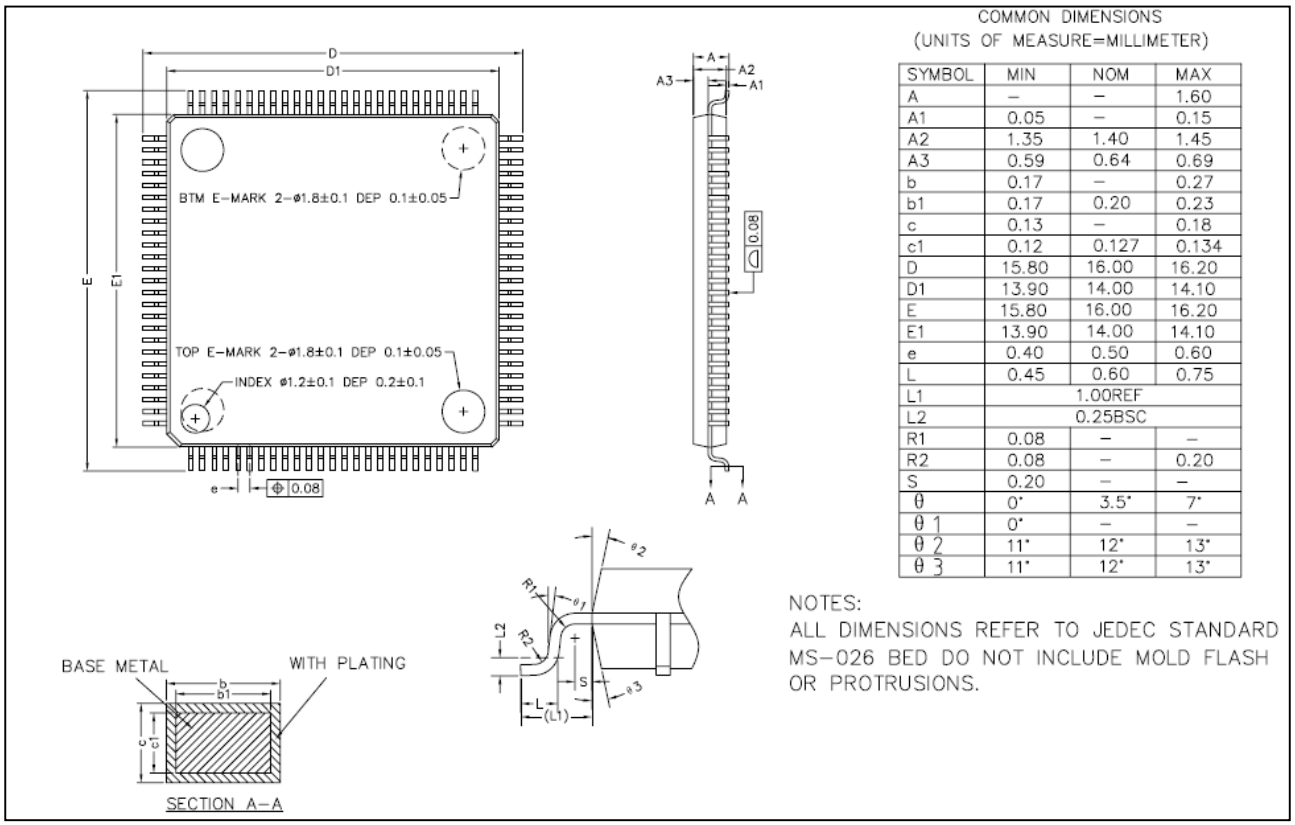
5.3 LQFP100

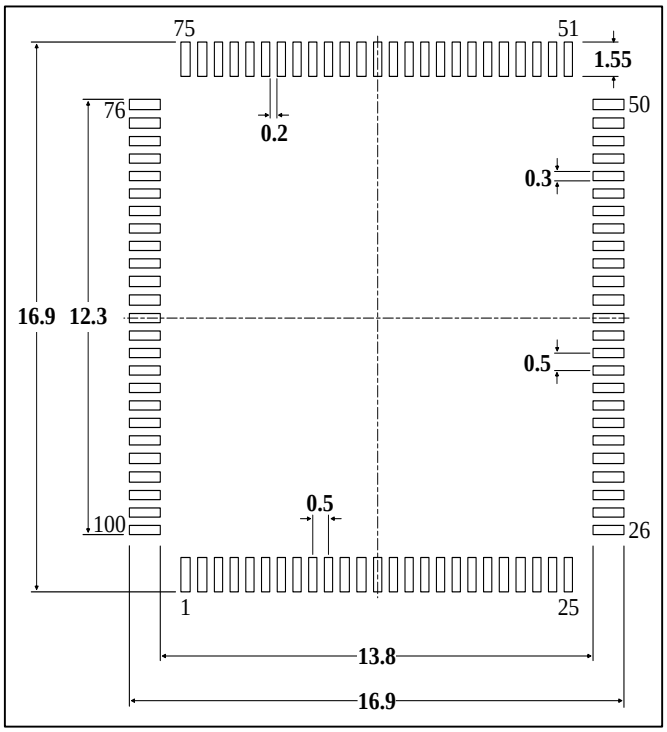
Figure 5-5 LQFP100 package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

Figure 5-6 LQFP100 recommended footprint (1)



1. Dimensions are expressed in millimeters.

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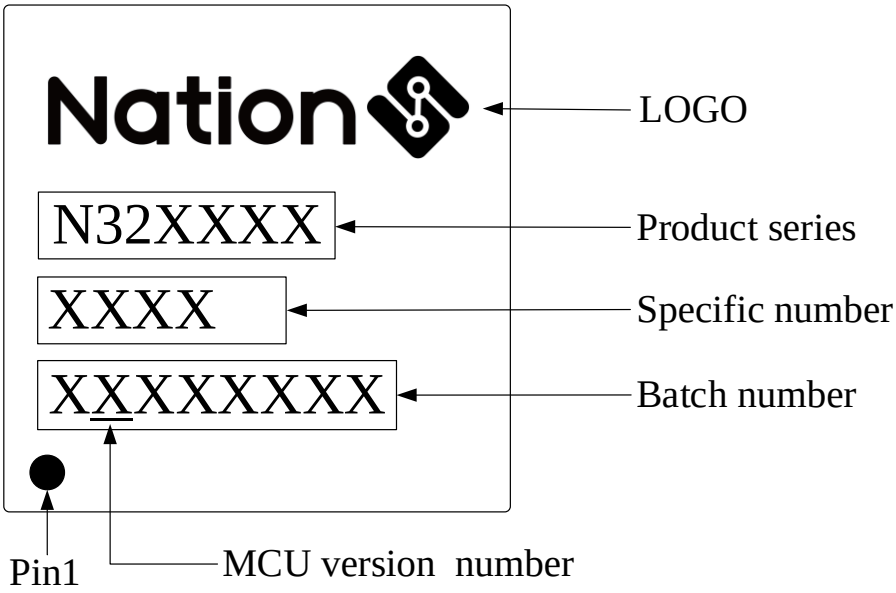
5.4 Marking Information

Figure 5-7 LQFP48/LQFP64/LQFP100 marking information



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6 Ordering information

Figure 6-1 N32A455 Series Part Number Information

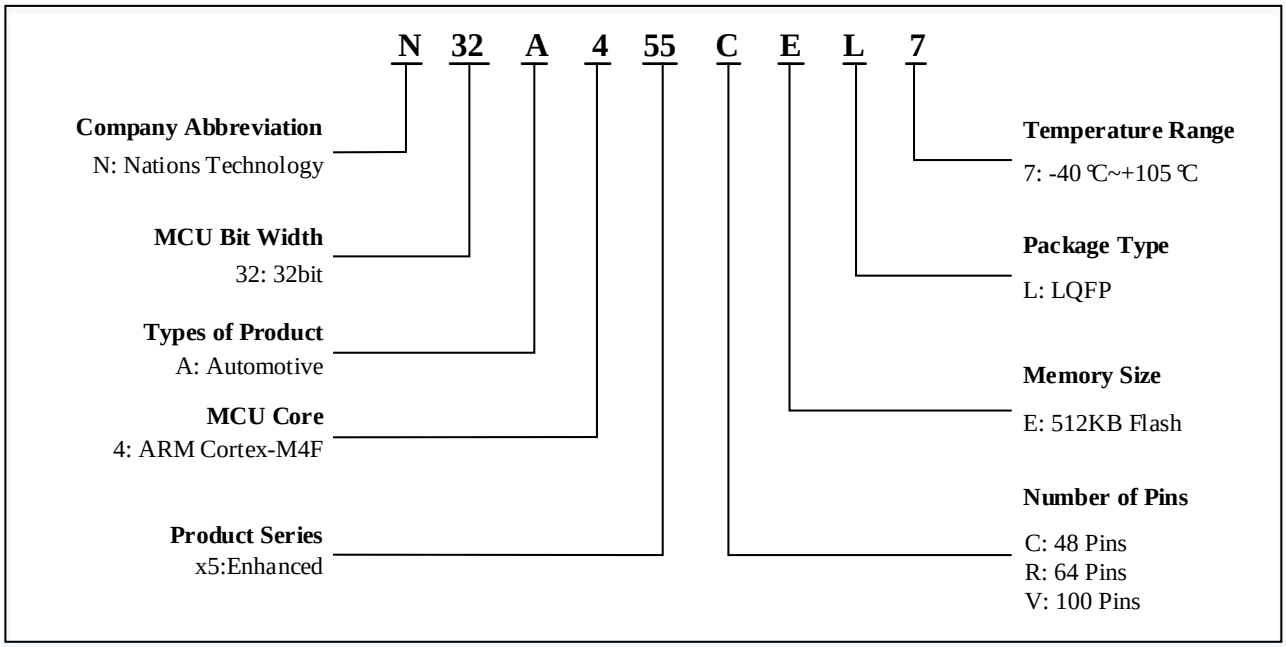

Table 6-1 N32A455 Series Ordering Code

Ordering code (1)	Package	Package size	Packaging (2)	SPQ(3)	Temperature range
N32A455CEL7	LQFP48	7mm*7mm	Tray	250	-40℃ ~ 105℃
N32A455REL7	LQFP64	10mm*10mm	Tray	160	-40℃ ~ 105℃
N32A455VEL7	LQFP100	14mm*14mm	Tray	90	-40℃ ~ 105℃

1. For the latest detailed ordering information, please refer to the Selection Guide.
2. The packaging provided is the basic packaging. If user has any other requirements, please contact NSING.
3. Minimum packaging quantity.

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7 Version History

Date	Version	Modify
2023.09.18	V1.0.0	Initial version
2024.11.19	V1.1.0	1. Modify chapter 3.2, ADC highest sampling rate 2. Modify table 4-33, the minimum time for SDA data retention is 0 3. Chapter 5 Add recommended footprint 4. Add chapter 6 5. Delete Part number information chapter
2025.6.9	V1.2.0	1. Modify the description of section 2.10, high level wakes up standby mode. RTC wake up event cannot wake up standby mode 2. Modify section 2.4 clock tree 3. Modify section 3.2, delete PA6 COMP1_OUT multiplexing function, add notes
2025.03.17	v1.3.0	1. Modify the description in Section 4.3.5.1 to specify that the access time wait cycle for flash memory is based on SYSCLK. 2. Modify the description in the main features section to “single-cycle hardware multiply instruction”. 3. Modify Table 4-20

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