

N32G003x5

Product Brief

N32G003 series based on 32-bit ARM Cortex-M0, run up to 48MHz, up to 29.5KB embedded flash, 3KB SRAM, 1x12bit 1Msps ADC, 1xCOMP, 2xUART, 1xI2C, 1xSPI.

Key features

- **Core**
 - A 32-bit ARM Cortex-M0 core, Single-cycle hardware multiply instruction
 - Run up to 48MHz
- **Encrypted memory**
 - Up to 29.5KByte embedded Flash memory, data 100,000 cycling and 10 years retention
 - Up to 3KB SRAM
- **Power consumption mode**
 - Run mode: all peripherals are configurable
 - Stop mode: TIM6, IWDG can be configured to work, SRAM data is maintained, and all IO states are maintained
 - Power Down mode: All power supply off, support NRST, PA1_WKUP0, PA2_WKUP1 wake-up
- **Clock**
 - HSI: Internal high-speed RC OSC 48MHz/40MHz(optional)
 - LSI: Internal low-speed RC OSC 32KHz
 - MCO: Support 1-way clock output, configurable HSI or LSI clock output that can be divided.
- **Reset**
 - Support power-on/power-off/external pin reset
 - Support programmable low voltage detection and reset
 - Support watchdog reset, software reset
- **Communication interface**
 - 2xUART, which supports asynchronous mode, multiprocessor communication mode, single-wire half-duplex mode
 - 1xSPI, rate up to 12MHz
 - 1xI2C, rate up to 1MHz, which can be configured in master/slave mode
- **Analog interface**
 - 1x12bit 1Msps high-speed ADC , up to 9 external single-ended input channels and 1 internal channel connected to the 1.2V reference
 - 1xhigh-speed analog comparator, positive terminal input supports four adjustable dropout voltages of 0mV/100mV/200mV/ 300mV
- **Support up to 18 GPIOs that support multiplexing.**
- **1xBeeper, support complementary output**
- **Timer counter**

- 1x16-bit advanced timer counters, support input capture, output compare, each timer has 4 independent channels, 3 of which support 6 complementary PWM output
- 1x16-bit general purpose timer counters, each timer has 2 independent channels, supports input capture/output compare/PWM output
- 1x16-bit basic timer counter, supports STOP wake-up low-power mode
- 1x24-bit SysTick
- 1x12-bit Independent watchdog (IWDG)
- **Programming mode**
 - Support SWD online debugging interface
- **Security features**
 - CRC16 calculation
 - Support multiple read protection(RDP) levels (L0/L1/L2)
- **96-bit UID and 128-bit UCID**
- **Working conditions**
 - Operating Voltage Range: 2V~5.5V
 - Operating Temperature Range: -40°C~105°C
 - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
 - QFN20(3mm x 3mm)
 - TSSOP20(6.5mm x 4.4mm)
 - TSSOP20-1(6.5mm x 4.4mm)
 - SOP8(4.9mm x 3.9mm)

1 Part number information

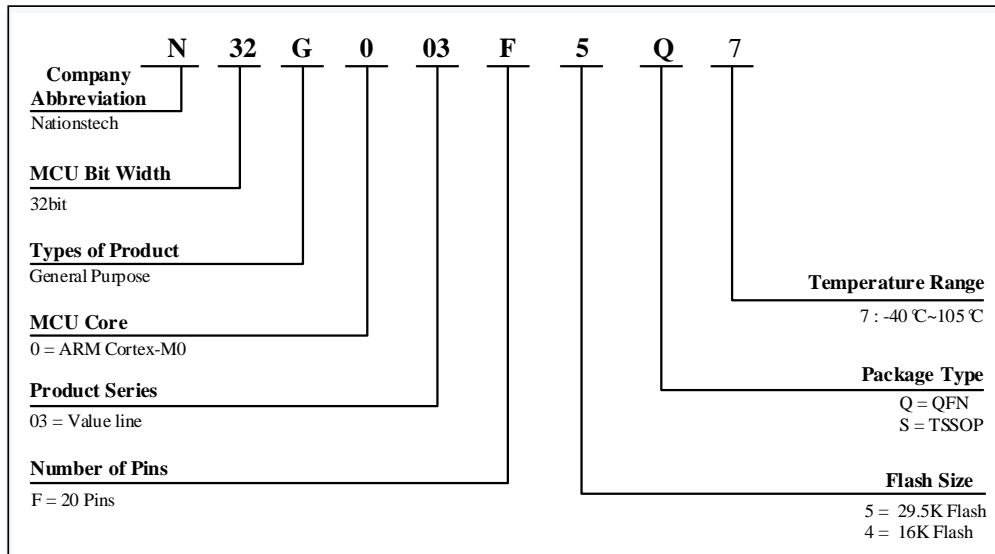


Table 1-1 N32G003 Series Ordering Code information

Ordering Code ⁽¹⁾	Package	Size	Packaging ⁽²⁾	SPQ ⁽³⁾	Temperature range
N32G003F5S7	TSSOP20	6.5mm x 4.4mm	Reel	70	-40°C~105°C
N32G003F5S7-1	TSSOP20-1	6.5mm x 4.4mm	Reel	70	-40°C~105°C
N32G003F5Q7	QFN20	3mm x 3mm	Tray	490	-40°C~105°C
N32G003F4S7	TSSOP20	6.5mm x 4.4mm	Reel	70	-40°C~105°C
N32G003F4Q7	QFN20	3mm x 3mm	Tray	490	-40°C~105°C
N32G003J5A7	SOP8	4.9mm x 3.9mm	Reel	100	-40°C~105°C

1. For the latest detailed ordering information, please refer to the selection manual.
2. This packaging is the basic packaging. If you have any other requirements, please contact Nsing Technology
3. Minimum packaging quantity

2 Product Model Resource Configuration

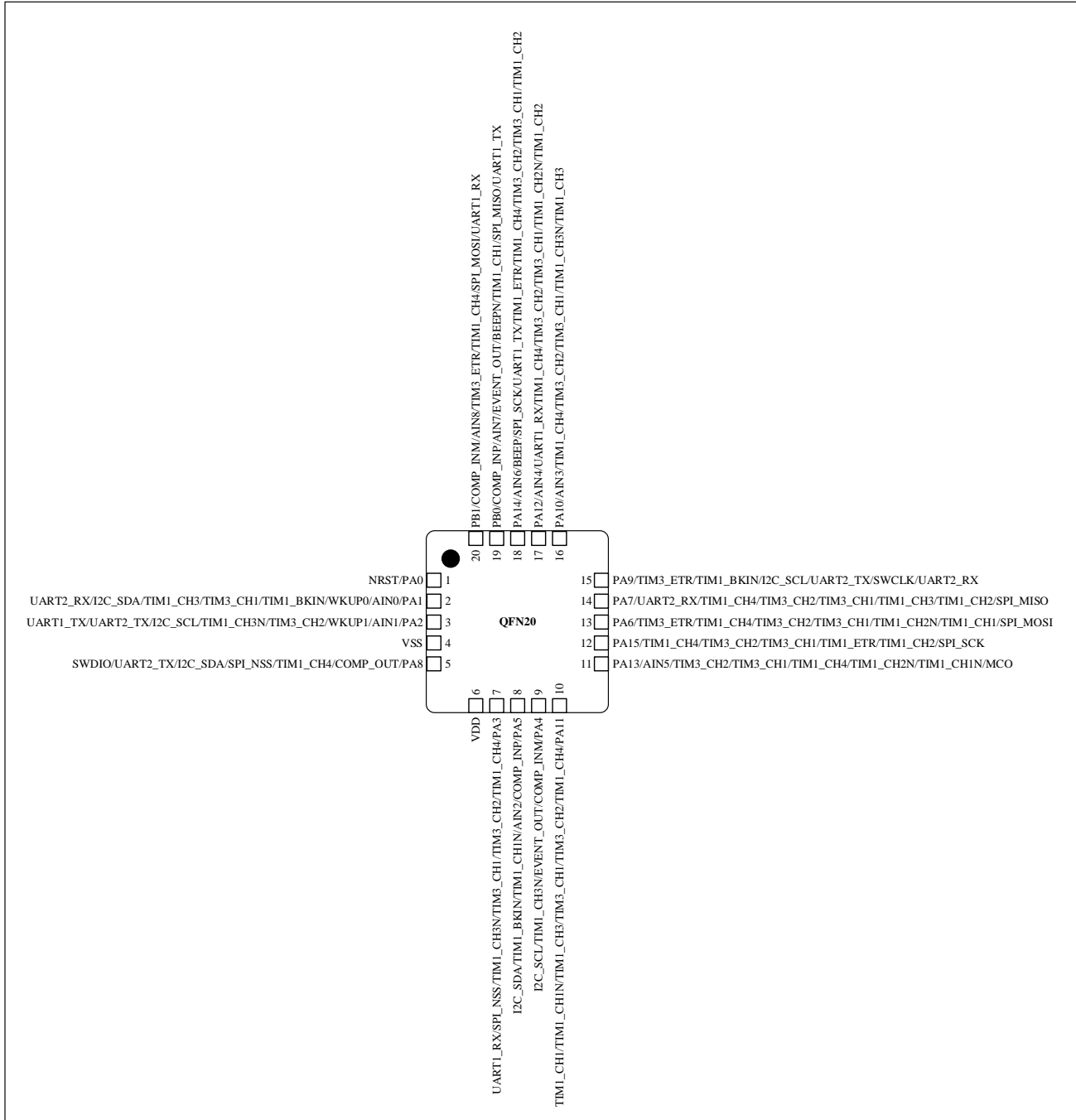
Table 2-1 N32G003 Series Resource Configuration

Part Number		N32G003J5A7	N32G003F5Q7/F4Q7	N32G003F5S7/F4S7	N32G003F5S7-1
Flash capacity (KB)		29.5	29.5/16	29.5/16	29.5
SRAM capacity (KB)		3	3	3	3
CPU frequency		ARM Cortex-M0 @ 48MHz			
Working environment		2~5.5V/-40~105°C			
Timer	General	1	1	1	1
	Advanced	1	1	1	1
	Basic	1	1	1	1
Communication interface	SPI	1	1	1	1
	I2C	1	1	1	1
	UART	2	2	2	2
GPIO		6	18		
12bit ADC		1x12bit	1x12bit	1x12bit	1x12bit
Number of channels		8Channel	9Channel	9Channel	9Channel
COMP		1	1	1	1
Beeper		1	1	1	1
Algorithm support		CRC16			
Security protection		Read protection (RDP)			
Package		SOP8	QFN20	TSSOP20	TSSOP20-1

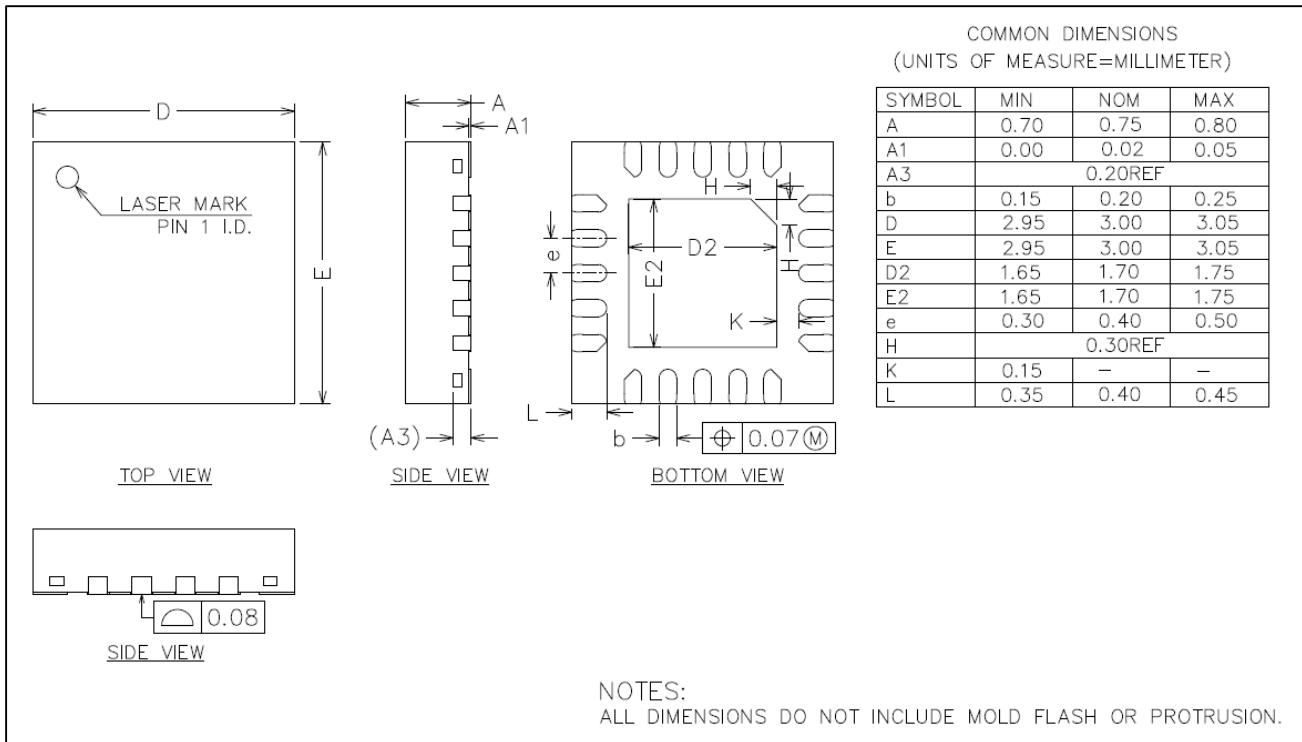
3 Package Information

3.1 QFN20

3.1.1 QFN20 Pinout

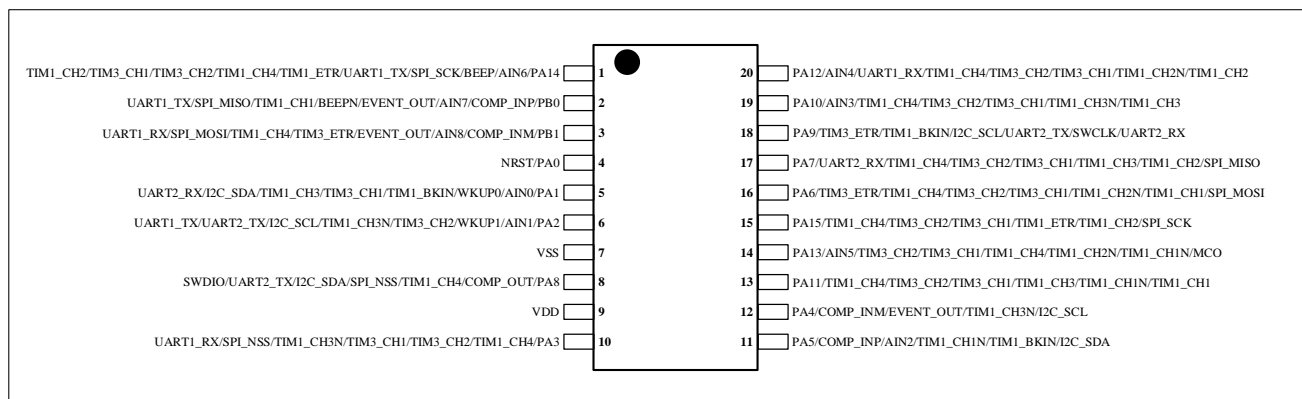


3.1.2 QFN20 Package

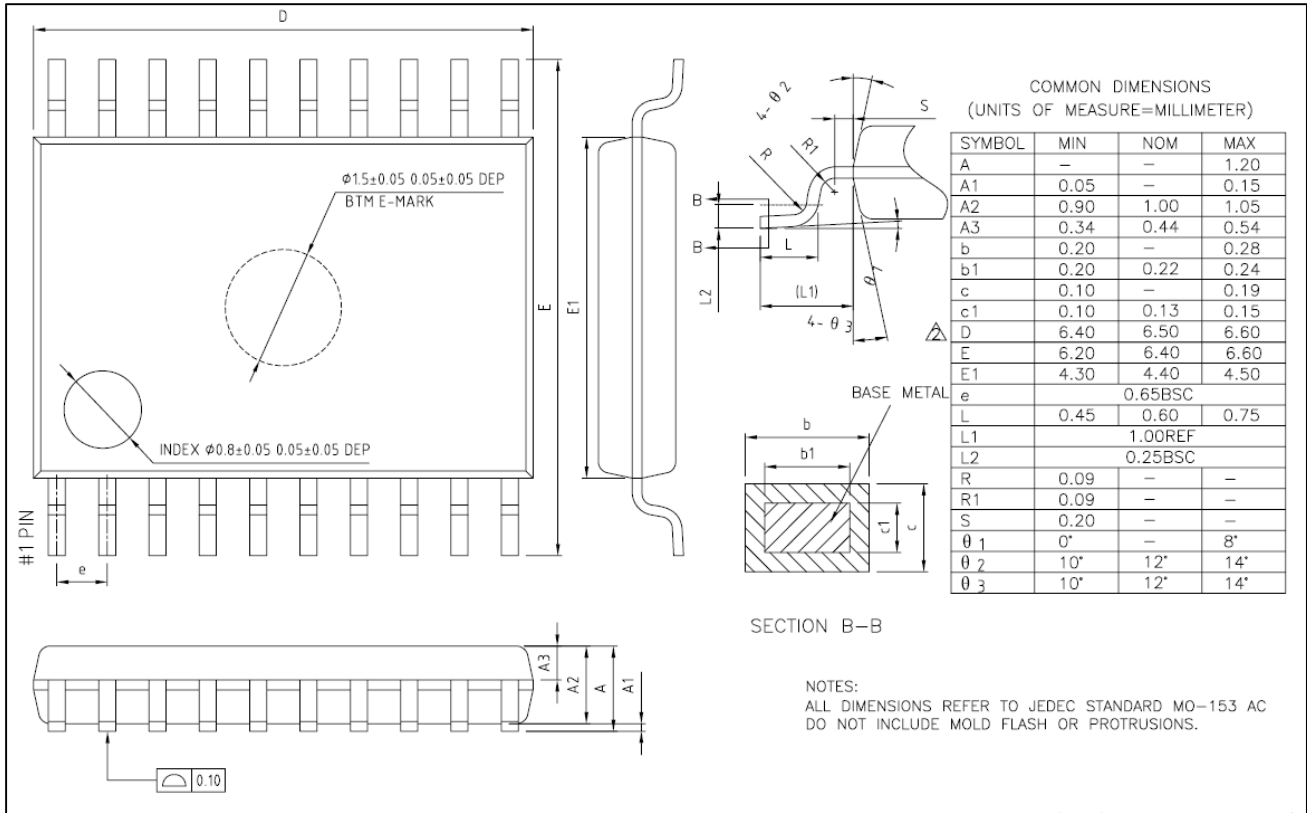


3.2 TSSOP20

3.2.1 TSSOP20 Pinout

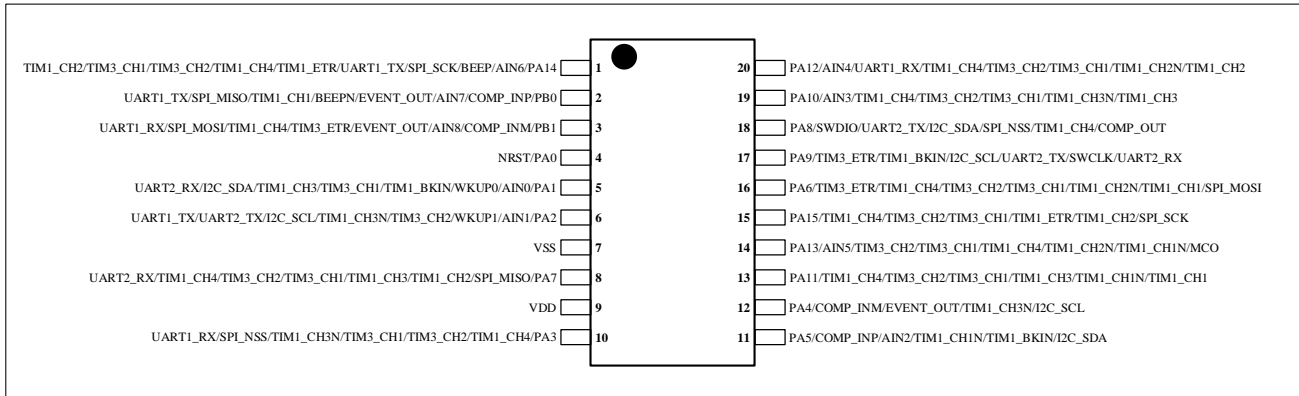


3.2.2 TSSOP20 Package

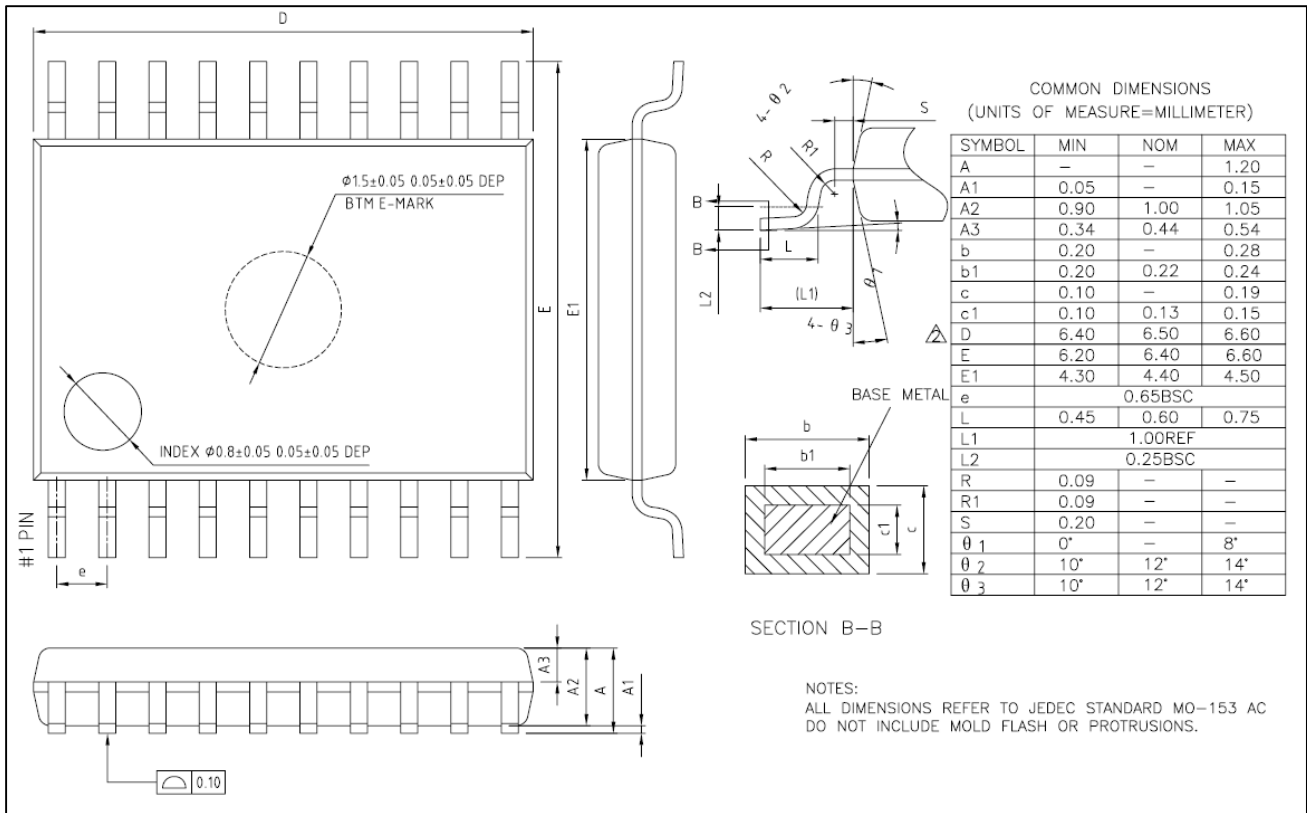


3.3 TSSOP20-1

3.3.1 TSSOP20-1 Pinout

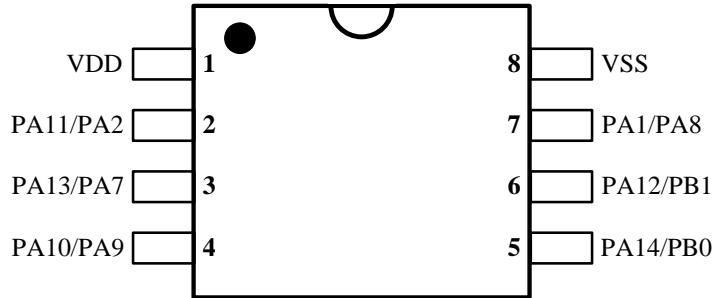


3.3.2 TSSOP20-1 Package



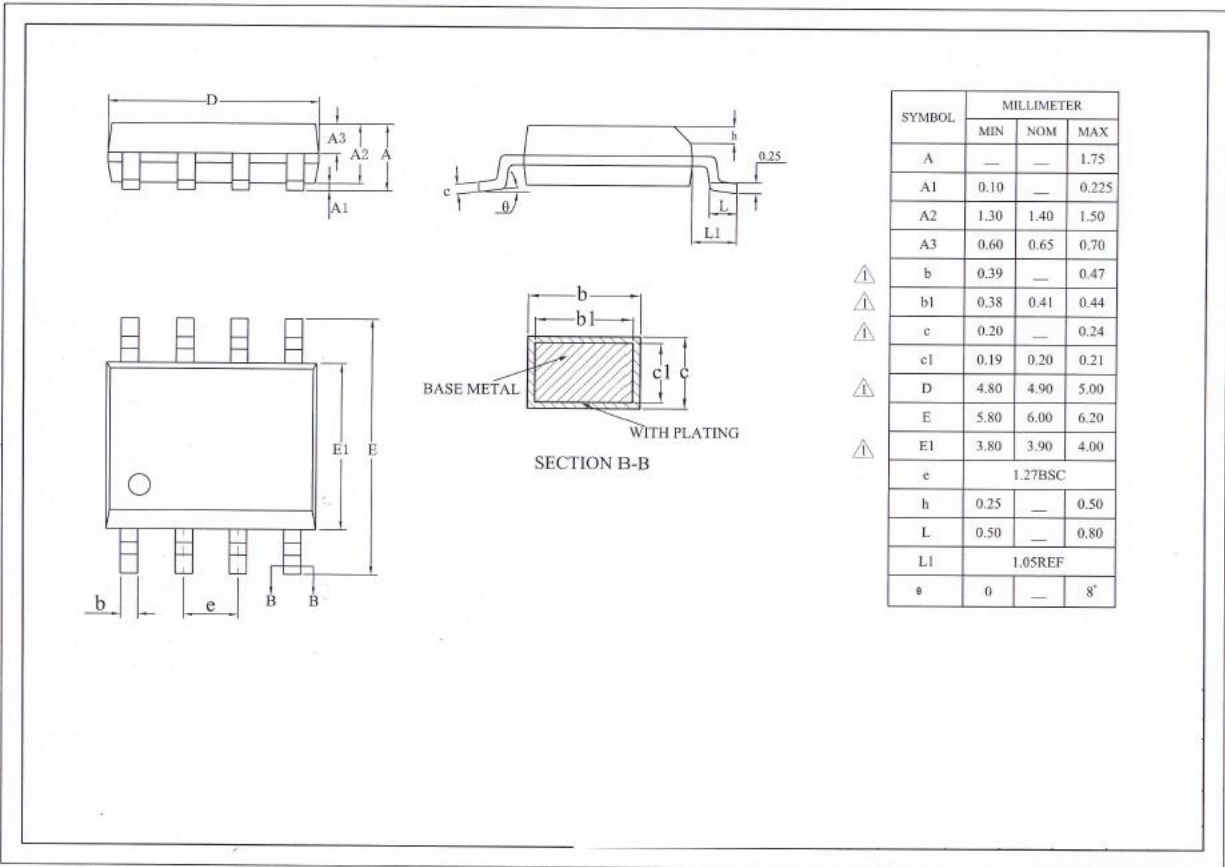
3.4 SOP8

3.4.1 SOP8 Pinout



1	VDD	
2	PA2	AIN1/WKUP1/TIM2_CH2/TIM1_CH3N/I2C_SCL/UART2_TX/UART1_TX
	PA11	TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH3/TIM1_CH1N/TIM1_CH1
3	PA7	UART2_RX/TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH3/TIM1_CH2/SPI_MISO
	PA13	AIN5/TIM2_CH2/TIM2_CH1/TIM1_CH4/TIM1_CH2N/TIM1_CH1N/MCO
4	PA9	TIM2_ETR/TIM1_BKIN/I2C_SCL/UART2_TX/SWCLK
	PA10	AIN3/TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH3N/TIM1_CH3
5	PA14	AIN6/BEEP/SPI_SCK/UART1_TX/TIM1_ETR/TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH2
	PB0	COMP_INP/AIN7/EVENT_OUT/BEEPN/TIM1_CH1/SPI_MISO/UART1_TX
6	PA12	AIN4/UART1_RX/TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH2N/TIM1_CH2
	PB1	COMP_INM/AIN8/EVENT_OUT/TIM2_ETR/TIM1_CH4/SPI_MOSI/UART1_RX
7	PA1	AIN0/WKUP0/TIM1_BKIN/TIM2_CH1/TIM1_CH3/I2C_SDA/UART2_RX
	PA8	COMP_OUT/TIM1_CH4/SPI_NSS/I2C_SDA/UART2_TX/SWDIO
8	VSS	

3.4.2 SOP8 Package



4 Version history

Date	Version	Remark
V1.0	2022.9.1	Initial release
V1.1.0	2023.7.14	1.Added N32G003F4S7\N32G003F4Q7 model chips 2.Modified pinout diagram: PA9 adds UART2_RX function
V1.2.0	2026.3.4	1.Add N32G003J5A7 and N32G003F5S7-1 2.Edit header and footer

5 Notice

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